



Technology and Service

SWITCHING REGULATOR ICs

DESIGNERS' DATAPACK

ADVANCED BIPOLAR ICs FROM THE SOURCE YOU CAN RELY ON.



SGS SWITCHING REGULATOR ICs

Already familiar to power supply designers as a major supplier of advanced linear regulators, SGS now offers the industry's most exciting range of switch-mode power supply ICs: industry standards such as the SG3524, leading-edge designs like the UC3840 and the remarkable L296 power switching regulator.

Behind this impressive range of products stands SGS' unrivalled experience in high volume production of advanced bipolar ICs, the same technological and production engineering expertise that made SGS the acknowledged leader in high power industrial and consumer circuits.

When you're looking for state-of-the-art products, high volume production capability and dependable technology call SGS, the source you can rely on.



quantum electronics

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Bramley

2018

SPECIAL LINEAR REGULATORS

L387/L487



Low drop 5V/500mA regulators with delayed reset function. L487 includes $\pm 80V$ load dump protection for automotive applications.

Fixed 500mA regulators available with 5V, 8.5V and 10V outputs. Include $\pm 100V$ load dump protection and need no external components.

L2600



L4700



Low drop 500mA regulators available in 5V, 8.5V and 10V versions. Feature 0.6V drop at 500mA and $\pm 80V$ load dump protection.

Very low drop 400mA regulators available in 5V, 8.5V and 10V versions. Feature 0.4V drop at 400mA, $\pm 60V$ load dump protection and foldback current limiter.

L4800



L4901



Dual 5V regulator (400mA output) with delayed reset for microprocessor systems

Fixed 8.5V/200mA regulator which includes a filter to provide high ripple rejection.

L4916



LM2930A LM2931A



Enhanced versions of LM2930 and LM2931 low drop 5V regulators with lower drop (0.2V at 150mA) and higher current (up to 400mA). Include load dump protection ($\pm 40V$ for LM2930A; $\pm 60V$ for LM2931A) and foldback current limiter.

Dual 5V regulator (750mA main and 10mA standby outputs) with very low drop and reset output. Reset output doubles as switch input for 750mA output.

LM2935

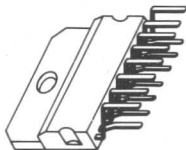


STANDARD LINEAR REGULATORS

SGS also manufactures a wide range of industry standard linear regulator types including the L7800, L7900, L78M00 and LM117 series. For detailed information see SGS' Voltage Regulators, Op amps and Comparators Databook.

SWITCHING REGULATORS

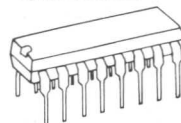
L296



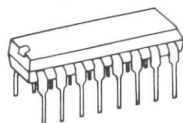
High power switching regulator delivering up to 4A at voltage variable from 5.1V to 40V. Operates very efficiently at switching frequencies to 200 kHz and includes current limiter, crowbar SCR control/driver, soft start, reset circuit and inhibit function.

Regulating pulse width modulator for single ended and push-pull applications. Includes current limiter and shutdown circuit.

SG3524



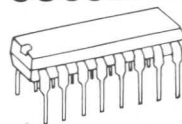
UC3524A



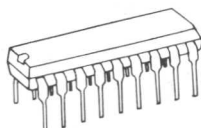
Advanced version of SG3524 with undervoltage lockout, PWM latch, improved current limiter, higher output current and precise $\pm 1\%$ reference.

Regulating pulse width modulators featuring 8-35V operation, wide oscillator range, sync terminal, adjustable deadtime control, soft start and dual source-sink drivers.

SG3525A **SG3527A**



UC3840



PWM controller for highly-efficient bootstrapped primary side operation in forward or flyback power converters. Incorporates many advanced features including pulse-by-pulse current limiting, current fault shutdown, latch-off or continuous retry after faults and duty cycle limiting.

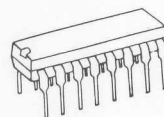
PRELIMINARY DATA

REGULATING PULSE WIDTH MODULATORS

- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT..8mA TYPICAL
- OPERATION UP TO 300 KHz
- 1% MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE

The SG1524, SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG1524 family was designed for switching regulators of either

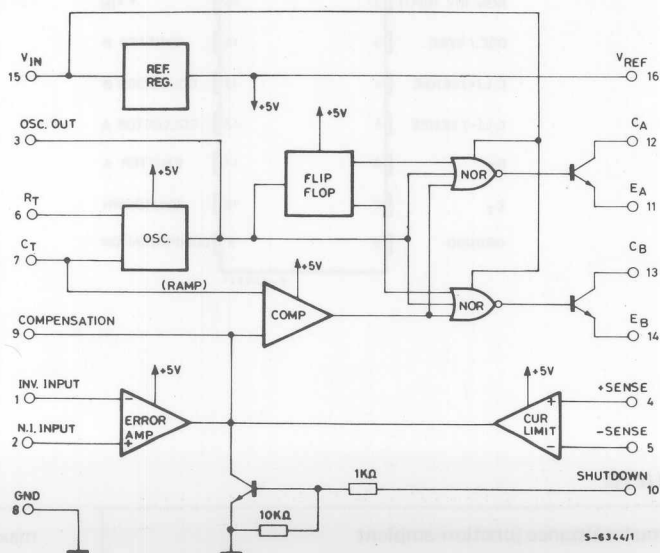
polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.



DIP-16

ORDERING NUMBERS: SG1524J - SG2524J - SG3524J (Ceramic)
SG2524N - SG3524N (Plastic)

BLOCK DIAGRAM



S-6344/1



SG1524
SG2524
SG3524

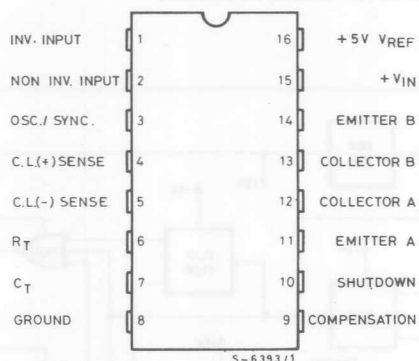


ABSOLUTE MAXIMUM RATINGS

V_{IN}	Supply voltage	40	V
I_C	Collector output current	100	mA
I_R	Reference output current	50	mA
I_T	Current through C_T terminal	-5	mA
P_{tot}	Total power dissipation at $T_{amb} = 70^\circ\text{C}$	1000	mW
T_{stg}	Storage temperature range	-65 to 150	$^\circ\text{C}$
T_{op}	Operating ambient temperature range	-55 to 125	$^\circ\text{C}$
		-25 to 85	$^\circ\text{C}$
		0 to 70	$^\circ\text{C}$



CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	$^\circ\text{C/W}$
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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_J = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for the SG1524, -25°C to $+85^{\circ}\text{C}$ for the SG2524, and 0°C to $+70^{\circ}\text{C}$ for the SG3524, $V_{IN} = 20\text{V}$, and $f = 20\text{KHz}$).

Parameter	Test condition	SG1524/SG2524			SG3524			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

REFERENCE SECTION

V_{REF}	Output Voltage		4.8	5	5.2	4.6	5	5.4	V
ΔV_{REF}	Line Regulation	$V_{IN} = 8$ to 40V		10	20		10	30	mV
ΔV_{REF}	Load Regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
	Ripple Rejection	$f = 120\text{Hz}$, $T_J = 25^{\circ}\text{C}$		66			66		dB
	Short Circuit Curr. Limit	$V_{REF} = 0$, $T_J = 25^{\circ}\text{C}$		100			100		mA
$\Delta V_{REF}/\Delta T$	Temp. Stability	Over Operating Temp. Range		0.3	1		0.3	1	%
ΔV_{REF}	Long Term Stability	$T_J = 25^{\circ}\text{C}$, $t = 1000$ Hrs.		20			20		mV

OSCILLATOR SECTION

f_{MAX}	Maximum Frequency	$C_T = 0.001\mu\text{F}$, $R_T = 2\text{k}\Omega$		300			300		kHz
	Initial Accuracy	R_T and C_T Constant		5			5		%
	Voltage Stability	$V_{IN} = 8$ to 40V , $T_J = 25^{\circ}\text{C}$			1			1	%
$\Delta f/\Delta T$	Temperature Stability	Over Operating Temp. Range			2			2	%
	Output Amplitude	Pin 3, $T_J = 25^{\circ}\text{C}$		3.5			3.5		V
	Output Pulse Width	$C_T = 0.01\mu\text{F}$, $T_J = 25^{\circ}\text{C}$		0.5			0.5		μs

ERROR AMPLIFIER SECTION

V_{os}	Input Offset Voltage	$V_{CM} = 2.5\text{V}$		0.5	5		2	10	mV
I_b	Input Bias Current	$V_{CM} = 2.5\text{V}$		2	10		2	10	μA
G_V	Open Loop Volt. Gain		72	80		60	80		dB
CMV	Common Mode Volt.	$T_J = 25^{\circ}\text{C}$	1.8		3.4	1.8		3.4	V
CMR	Comm. Mode Rejec.	$T_J = 25^{\circ}\text{C}$		70			70		dB
B	Small Signal Bandwidth	$A_V = 0\text{dB}$, $T_J = 25^{\circ}\text{C}$		3			3		MHz
V_o	Output Voltage	$T_J = 25^{\circ}\text{C}$	0.5		3.8	0.5		3.8	V

COMPARATOR SECTION

	Duty-Cycle	% Each Output On	0		45	0		45	%
V_{IT}	Input Threshold	Zero Duty-Cycle		1			1		V
V_{IT}	Input Threshold	Maximum Duty-Cycle		3.5			3.5		V
I_b	Input Bias Current			1			1		μA

CURRENT LIMITING SECTION

	Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max. Out, $T_J = 25^{\circ}\text{C}$	190	200	210	180	200	220	mV
	Sense Voltage T.C.			0.2			0.2		$\text{mV}/^{\circ}\text{C}$
CMV	Common Mode Volt.		-1		+1	-1		+1	V

OUTPUT SECTION (Each Output)

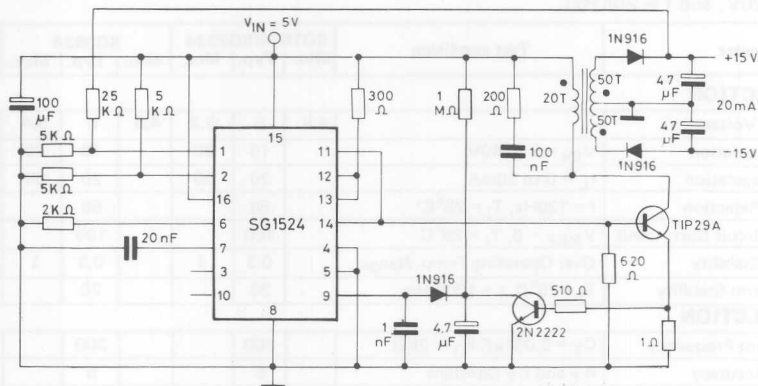
	Collector-Emitter Volt.		40			40			V
	Collector Leakage Cur.	$V_{CE} = 40\text{V}$		0.1	50		0.1	50	μA
	Saturation Voltage	$I_C = 50\text{mA}$		1	2		1	2	V
	Emitter Out. Voltage	$V_{IN} = 20\text{V}$	17	18		17	18		V
t_r	Rise Time	$R_C = 2\text{k}\Omega$, $T_J = 25^{\circ}\text{C}$		0.2			0.2		μs
t_f	Fall time	$R_C = 2\text{k}\Omega$, $T_J = 25^{\circ}\text{C}$		0.1			0.1		μs
I_q^*	Total Standby Curr.	$V_{IN} = 40\text{V}$		8	10		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.



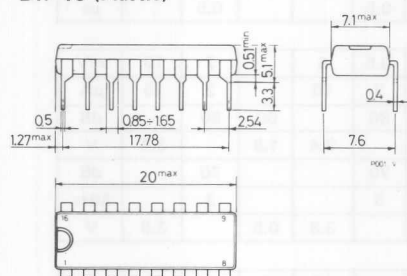
SG1524
SG2524
SG3524

Fig. 8 - Flyback converter circuit

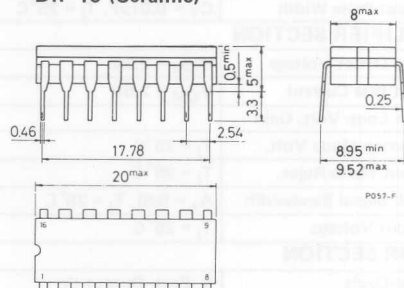


MECHANICAL DATA (Dimension in mm)

DIP 16 (Plastic)



DIP 16 (Ceramic)



part out of
SEQUENCE

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Fig. 1 - Open-loop voltage amplification of error amplifier vs. frequency.

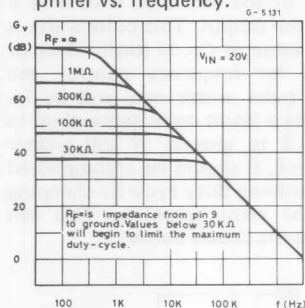


Fig. 2 - Oscillator frequency vs. timing components.

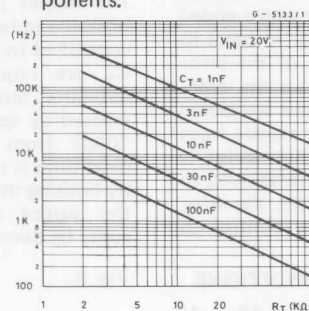


Fig. 3 - Output dead time vs. timing capacitance value.

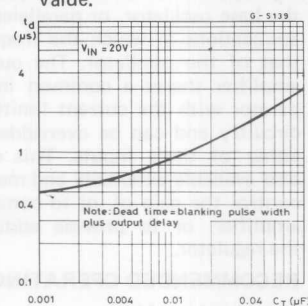


Fig. 4 Output saturation voltage vs. load current.

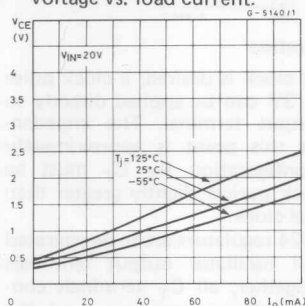
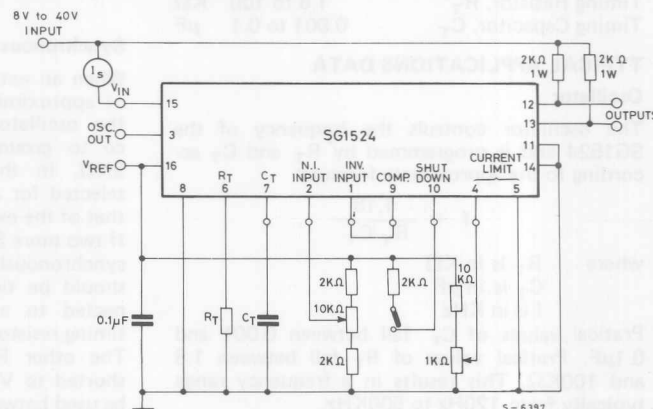


Fig. 5 - Open loop test circuit.



PRINCIPLES OF OPERATION

The SG1524 is a fixed-frequency pulse-with-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T established a constant charging current for C_T . This results in a linear voltage ramp at C_T , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG1524 contains, an on-board 5V regulator that serves as a reference as well as powering the SG1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode

range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T . The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (Q_A or Q_B) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T . The

outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{IN}	8 to 40	V
Reference Output Current	0 to 20	mA
Current through C_T Terminal	-0.03 to -2	mA
Timing Resistor, R_T	1.8 to 100	K Ω
Timing Capacitor, C_T	0.001 to 0.1	μ F

TYPICAL APPLICATIONS DATA

Oscillator

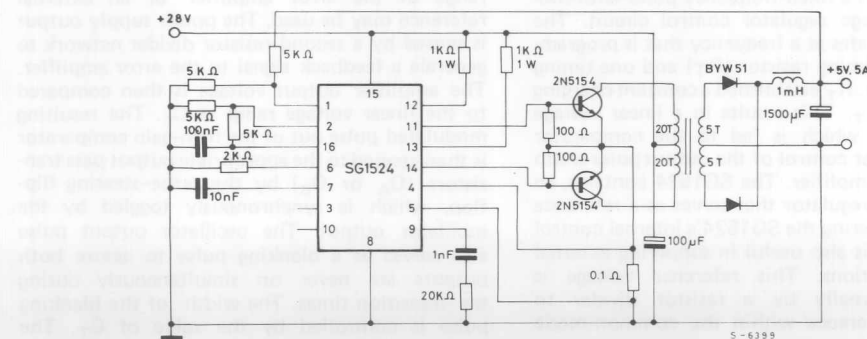
The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T according to the approximate formula:

$$f \approx \frac{1.18}{R_T C_T}$$

where R_T is in K Ω
 C_T is in μ F
 f is in KHz

Practical values of C_T fall between 0.001 and 0.1 μ F. Practical values of R_T fall between 1.8 and 100 K Ω . This results in a frequency range typically from 120Hz to 500KHz.

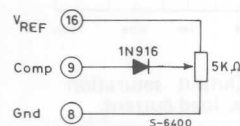
Fig. 7 - Push-pull transformer-coupled circuit.



Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T . If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

Fig. 6



Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2K Ω . In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF} . Minimum lead lengths should be used between the C_T terminals.



PRELIMINARY DATA

PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

- ALL CONTROL, DRIVING, MONITORING, AND PROTECTION FUNCTIONS INCLUDED
- LOW-CURRENT, OFF-LINE START CIRCUIT
- FEED-FORWARD LINE REGULATION OVER 4 TO 1 INPUT RANGE
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- PULSE-BY-PULSE CURRENT LIMITING PLUS SHUTDOWN FOR OVER-CURRENT FAULT
- NO START-UP OR SHUTDOWN TRANSIENTS
- SLOW TURN-ON AND MAXIMUM DUTY-CYCLE CLAMP
- SHUTDOWN UPON OVER- OR UNDER-VOLTAGE SENSING
- LATCH OFF OR CONTINUOUS RETRY AFTER FAULT
- REMOTE, PULSE-COMMANDABLE START/STOP
- PWM OUTPUT SWITCH USABLE TO 1A PEAK CURRENT
- 1% REFERENCE ACCURACY
- 500 kHz OPERATION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over

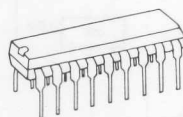
a wide input voltage range.

In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

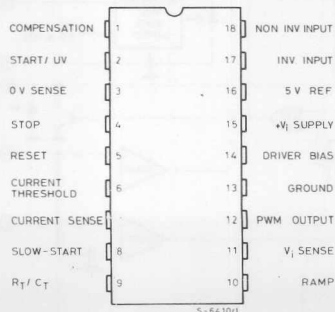
The UC1840 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2840 and UC3840 are designed for operation from -25°C to +85°C and 0°C to +70°C, respectively.



DIP-18

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Type	Plastic	Ceramic
UC1840	UC1840N	UC1840J
UC2840	UC2840N	UC2840J
UC3840	UC3840N	UC3840J



UC1840
UC2840
UC3840

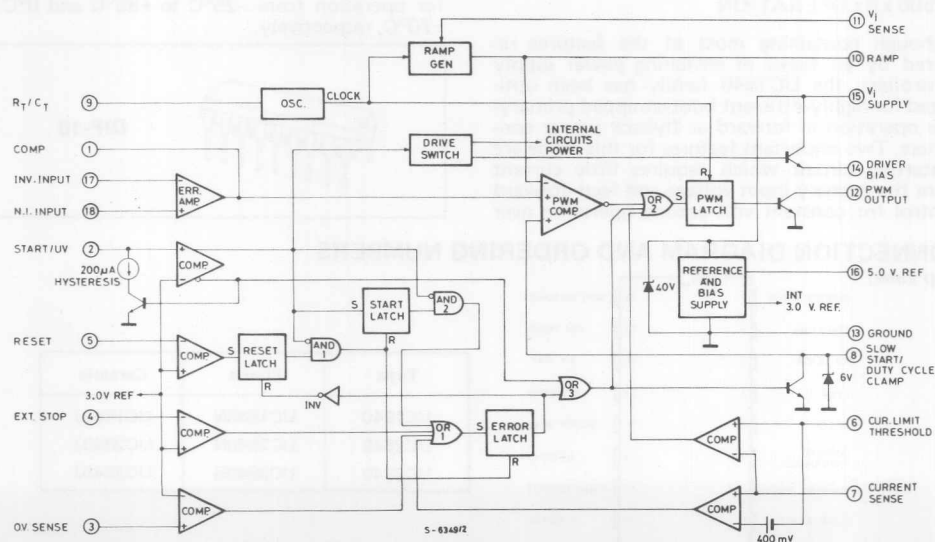
LINEAR
INTEGRATED
CIRCUITS



ABSOLUTE MAXIMUM RATINGS

V_i	Supply voltage + V_i (pin 15)		
	Voltage driven	32	V
	Current driven 100 mA maximum	self limiting	
V_o	PWM output voltage (pin 12)	40	V
I_o	PWM output current, steady-state (pin 12)	400	mA
E_{op}	PWM output peak energy discharge	20	μ J
	Driver bias current (pin 14)	-200	mA
$I_{o(REF)}$	Reference output current (pin 16)	-50	mA
	Slow start sink current (pin 8)	20	mA
	V_i sense current (pin 11)	10	mA
	Current limit inputs (pin 6, 7)	-0.5 to +5.5	V
	Comparator inputs (pins 2, 3, 4, 5, 17, 18)	-0.3 to +32	V
P_{tot}	Power dissipation at $T_{amb} = 70^\circ\text{C}$	1000	mW
T_j	Junction temperature range	-55 to 150	$^\circ\text{C}$
T_{op}	Operating ambient temperature range: UC1840	-55 to 125	$^\circ\text{C}$
	UC2840	-25 to 85	$^\circ\text{C}$
	UC3840	0 to 70	$^\circ\text{C}$
T_{stg}	Storage temperature	-65 to +150	$^\circ\text{C}$

BLOCK DIAGRAM





UC1840
UC2840
UC3840

THERMAL DATA

$R_{th\ j-amb}$ Thermal resistance junction-ambient	max 80 °C/W
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FUNCTIONAL DESCRIPTION

Name	Function
PWM CONTROL	
OSCILLATOR	Generates a fixed-frequency internal clock from an external R_T and C_T . $\text{Frequency} = \frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
RAMP GENERATOR	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R} \cdot C_R$ is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
ERROR AMPLIFIER	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance: unity-gain stable.
REFERENCE GENERATOR	Precision 5.0V for internal and external usage to 50 mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm 2\%$. 40V clamp zener for chip O.V. protection, 100mA maximum current.
PWM COMPARATOR	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
PWM LATCH	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
PWM OUTPUT SWITCH	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.



UC1840
UC2840
UC3840

FUNCTIONAL DESCRIPTION (continued)

Name

Function

SEQUENCING FUNCTIONS

START/U.V. SENSE

This comparator performs three functions.
With an increasing voltage, it generates a turn-on signal at a start threshold.
With a decreasing voltage, it generates a U.V. fault signal at a lower level separated by a 200 μ A hysteresis current.
At the U.V. threshold, it also resets the Error Latch if the Reset Latch has been set.

DRIVE SWITCH

Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.

DRIVE BIAS

Supplies drive current to external power switch to provide turn-on bias.

SLOW START

Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_s C_s$ for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider $R_s R_{DC}$.

START LATCH

Keeps low input voltage at initial turn-on from being defined as a U.V. fault. Sets at start level to monitor for U.V. fault.

RESET LATCH

When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off.
When set, this latch resets the Start and Error latches at the U.V. low threshold, allowing a restart.

PROTECTION FUNCTIONS

ERROR LATCH

When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset.

Inputs to Error Latch are:

- U.V. low (after turn-on)
- O.V. high
- Step low
- Current Sense 400mV over threshold.

Error Latch resets at U.V. threshold if Reset Latch is set.

CURRENT LIMITING

Differential input comparator terminates individual output pulses each time sense voltage rises above threshold.

When sense voltage rises to 400 mV above threshold, a shutdown signal is sent to Error Latch.



UC1840
UC2840
UC3840

ELECTRICAL CHARACTERISTICS (Refer to the test circuit. Unless otherwise stated, these specifications apply for $T_j = -55$ to $+125^\circ\text{C}$ for the UC1840, -25°C to $+85^\circ\text{C}$ for the UC2840 and 0 to 70°C for the UC3840; $V_i = 20\text{V}$, $R_T = 20\text{K}\Omega$, $C_T = 0.001\text{ }\mu\text{F}$, $C_R = 0.001\text{ }\mu\text{F}$, current limit threshold = 200mV)

Parameter	Test conditions	UC1840 UC2840			UC3840			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	

POWER INPUTS

I_{ST}	Start-up current	$V_i = 30\text{V}$, Pin 2 = 2.5V , $T_j = 25^\circ\text{C}$		4	5.5		4	5.5	mA
	*Start-up current T.C.	$V_i = 30\text{V}$, Pin 2 = 2.5V		-0.1	-0.2		-0.1	-0.2	%/ $^\circ\text{C}$
I_i	Operating current	$V_i = 30\text{V}$, Pin 2 = 3.5V	5	10	15	5	10	15	mA
V_{SOV}	Supply O.V. clamp	$I_i = 20\text{mA}$	33	40	45	33	40	48	V

REFERENCE SECTION

V_{REF}	Reference voltage	$T_j = 25^\circ\text{C}$	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line regulation	$V_i = 8$ to 30V		10	15		10	20	mV
ΔV_{REF}	Load regulation	$I_L = 0$ to 20mA		10	20		10	30	mV
$\Delta V_{REF}/\Delta T$	* Temperat. coeff.	Over op. temp. range			± 0.4			± 0.4	mV/ $^\circ\text{C}$
I_{SC}	Short circuit curr.	$V_{REF} = 0$, $T_j = 25^\circ\text{C}$		-80	-100		-80	-100	mA

OSCILLATOR

f_s	Nominal frequency	$T_j = 25^\circ\text{C}$	47	50	53	45	50	55	KHz
	Voltage stability	$V_i = 8$ to 30V		0.5	1		0.5	1	%
	* Temperature coeff.	Over op. temp. range			± 0.8			± 0.8	%/ $^\circ\text{C}$
$f_{s(max)}$	Maxim. frequency	$R_T = 2\text{K}\Omega$, $C_T = 330\text{pF}$	500			500			KHz

RAMP GENERATOR

	Ramp current min.	$I_{SENSE} = -10\text{ }\mu\text{A}$		-11	-14		-11	-14	μA
	Ramp current max.	$I_{SENSE} = 1\text{mA}$	-0.9	-0.95		-0.9	-0.95		mA
	Ramp valley		0.3	0.5	0.7	0.3	0.5	0.7	V
	Ramp peak	Clamping level	3.9	4.2	4.5	3.9	4.2	4.5	V

ERROR AMPLIFIER

V_{OS}	Input offset voltage	$V_{CM} = 5\text{V}$		0.5	5		2	10	mV
I_b	Input bias current			0.5	2		1	5	μA
I_{OS}	Input offset current				0.5			0.5	μA
G_v	Open loop gain	$\Delta V_O = 1$ to 3V	60	66		60	66		dB
	Output swing (max Out $\leq$ Ramp peak -100mV)	Minimum total range	0.3		3.5	0.3		3.5	V
CMR	Common mode rejection	$V_{CM} = 1.5$ to 5.5V	70	80		70	80		dB
SVR	Supply voltage rejection	$V_i = 8$ to 30V	40	50		40	50		dB



UC1840
UC2840
UC3840

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{SC}	Short circuit curr.	V _{comp} = 0V		-4	-10		-4	-10	mA
B*	Gain bandwidth	T _j = 25°C, G _V = 0 dB	1	2		1	2		MHz
SR*	Slew rate	T _j = 25°C, G _V = 0 dB		0.8			0.8		V/μs

PWM SECTION

	* Continuous duty cycle range (other than zero)	Min. total cont. range Ramp peak < 4.2V	5		95	5		95	%
$V_{O(sat)}$	Output saturation	$I_O = 20\text{ mA}$		0.2	0.4		0.2	0.4	V
$V_{O(sat)}$	Output saturation	$I_O = 200\text{ mA}$		1.7	2.2		1.7	2.2	V
I_{OL}	Output leakage	$V_O = 40V$		0.1	10		0.1	10	μA
τ_d	* Comparator delay	Pin 8 to pin 12 $T_j = 25^\circ C, R_L = 1\text{ K}\Omega$		300	500		300	500	ns

SEQUENCING FUNCTIONS

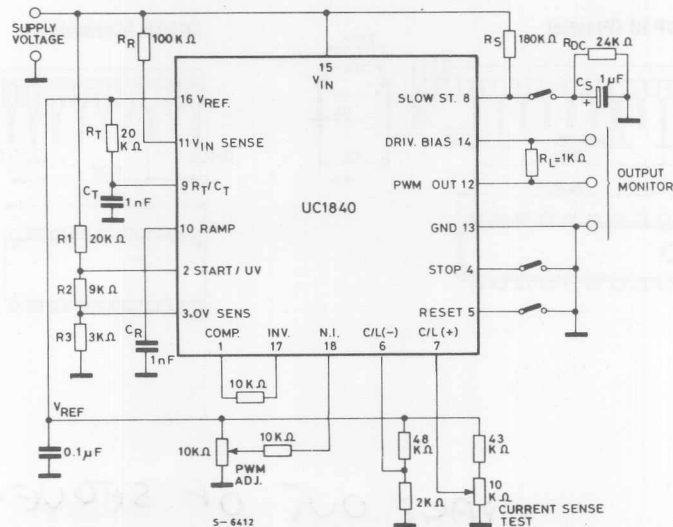
V_T	Comparator threshold	Pins 2, 3, 4, 5	2.8	3	3.2	2.8	3	3.2	V
I_b	Input bias current	Pins 3, 4, 5 = 0V		-1	-3		-1	-3	μA
	Start/UV Hysteresis current	Pin 2 = 2.5V, $T_j = 25^\circ C$	180	200	220	170	200	230	μA
	Input leakage	$V_i = 20V$		0.1	10		0.1	10	μA
	Driver bias saturation voltage $V_{IN}-V_{OH}$	$I_B = -50\text{ mA}$		2	3		2	3	V
	Driver bias leakage	$V_B = 0V$		-0.1	-10		-0.1	-10	μA
	Slow-start saturat.	$I_s = 2\text{ mA}$		0.2	0.5		0.2	0.5	V
	Slow-start leakage	$V_s = 4.5V$		0.1	2		0.1	2	μA

CURRENT CONTROL

	Current limit offset			0	5		0	10	mV
	Current shutdown offset		370	400	430	360	400	440	mV
I_b	Input bias current	Pin 7 = 0V		-2	-5		-2	-5	μA
	* Common mode range		-0.4		3	-0.4		3	V
τ_d^*	Current limit delay	$T_j = 25^\circ C, \text{ Pin 7 to 12, } R_L = 1\text{ K}\Omega$		200	400		200	400	ns

* Guaranteed by design. Not 100% tested in production.

Fig. 1 - Open loop test circuit



$$\text{Nominal frequency} = \frac{1}{R_T C_T} = 50 \text{ kHz}$$

$$\text{Start voltage} = 3 \left(\frac{R_1 + R_2 + R_3}{R_2 + R_3} \right) + 0.2 R_1 = 12V$$

$$\text{U.V. fault voltage} = 3 \left(\frac{R_1 + R_2 + R_3}{R_2 + R_3} \right) = 8V$$

$$\text{O.V. fault voltage} = 3 \left(\frac{R_1 + R_2 + R_3}{R_3} \right) = 32V$$

Current limit = 200 mV
Current fault voltage = 600 mV
Duty cycle clamp = 50%

Fig. 2 - Start U.V. hysteresis current

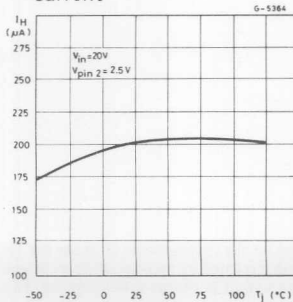


Fig. 3 - PWM Output saturation voltage

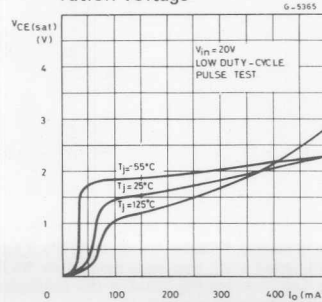
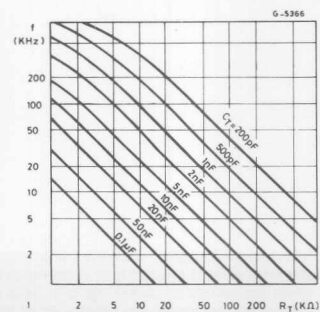


Fig. 4 - Oscillator frequency

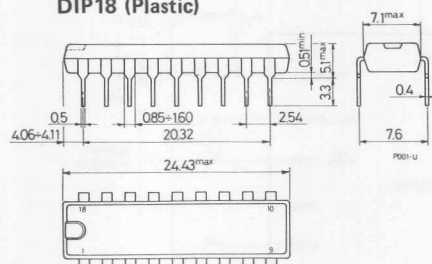




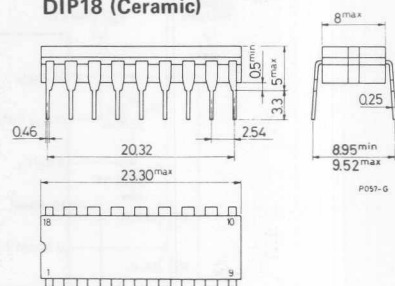
UC1840
UC2840
UC3840

MECHANICAL DATA (Dimensions in mm)

DIP18 (Plastic)



DIP18 (Ceramic)



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Fig. 5 - PWM output minimum pulse width

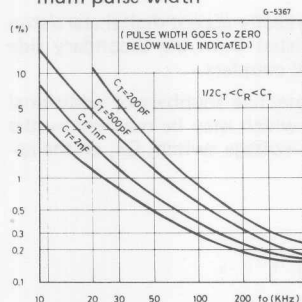


Fig. 6 - Error amplifier open-loop gain and phase

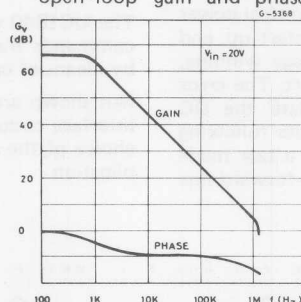
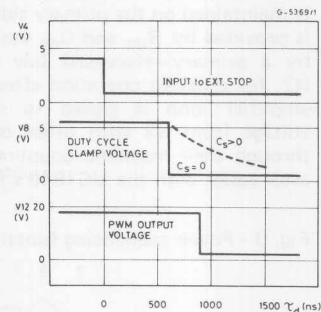
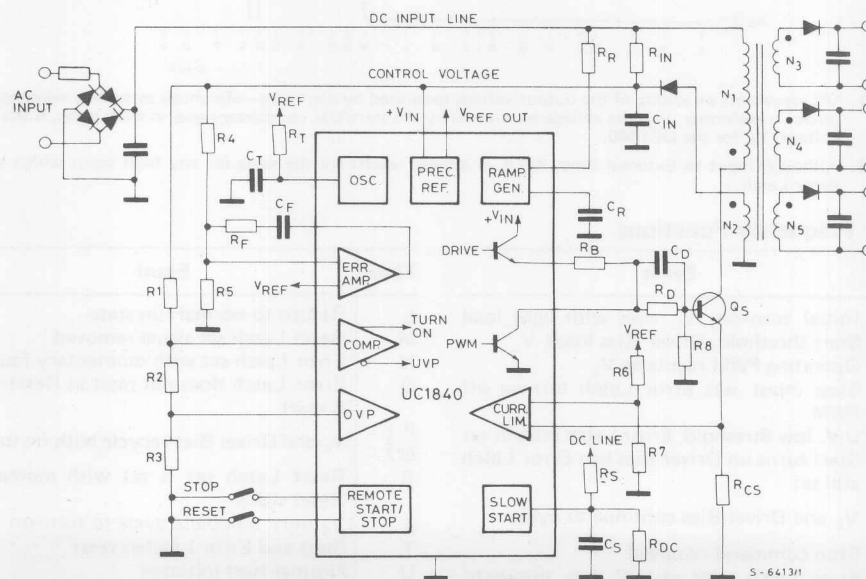


Fig. 7 - Shutdown timing



APPLICATION INFORMATION

Fig. 8 - Programmable PWM controller in a simplified flyback regulator





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UC3840

APPLICATION INFORMATION (continued)

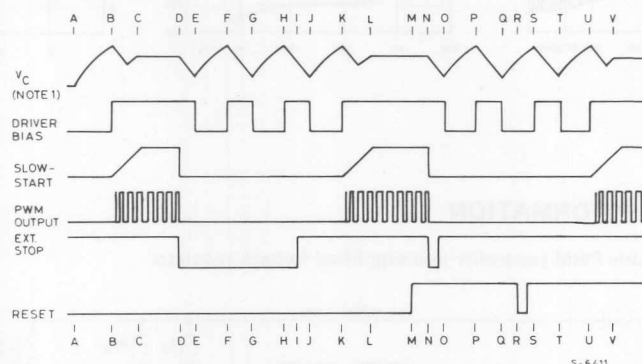
In this application (see Fig. 8) complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1840's feed-forward line

regulation.

The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Q_s , or the application.

Fig. 9 - Power sequencing functions



- Notes:**
1. V_c represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/U.V. comparator and, in most cases, is the supply voltage, V_i , for the UC1840.
 2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

Power Frequency Functions

Time	Event	Time	Event
A	Initial turn-on, V_c rises with light load	L	Return to normal run state
B	Start threshold. Driver Bias loads V_c	M	Reset Latch set signal removed
C	Operating PWM regulates V_c	N	Error Latch set with momentary fault
D	Stop input sets Error Latch turning off PWM	O	Error Latch does not reset as Reset Latch is reset
E	U.V. low threshold. Error Latch remain set	P } Q }	V_c and Driver Bias recycle with no turn-on
F	Start turns on Driver Bias bus Error Latch still set	R	Reset Latch set is set with momentary Reset signal
G } H }	V_c and Driver Bias continue to cycle	S	V_c must complete cycle to turn-on
I	Stop command removed	T	Start and Error Latches reset
J	Error Latch reset at U.V. low threshold	U	Normal start initiated
K	Start threshold now removes slow-start clamp	V	Return to normal run state

PRELIMINARY DATA

ADVANCED REGULATING PULSE WIDTH MODULATORS

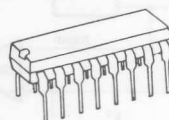
- FULLY INTERCHANGEABLE WITH SG1524
- PRECISION REFERENCE ($\pm 1\%$)
- HIGH-PERFORMANCE CURRENT LIMITER
- UNDER-VOLTAGE LOCKOUT WITH HYSTERETIC TURN-ON
- START-UP SUPPLY CURRENT LESS THAN 4mA
- OUTPUT CURRENT TO 200mA
- 60V OUTPUT CAPABILITY
- WIDE COMMON-MODE INPUT RANGE FOR BOTH ERROR AND CURRENT LIMIT AMPLIFIERS
- PWM LATCH INSURES SINGLE PULSE PER PERIOD
- 200ns SHUTDOWN THROUGH PWM LATCH
- GUARANTEED FREQUENCY ACCURACY
- THERMAL SHUTDOWN PROTECTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard SG1524 while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

The UC1524A includes a precise 5V reference trimmed to $\pm 1\%$ accuracy, eliminating the need for potentiometer adjustments, an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter free activation.

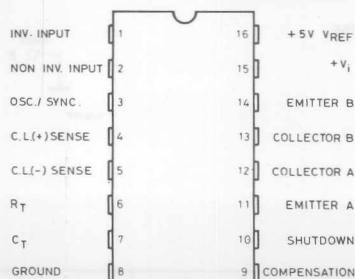
Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period even in noisy environments and a shutdown circuit feeding directly to the latch which will disable the outputs within 200ns. The oscillator circuit of the UC1524A is usable beyond 500KHz and is now easier to synchronize with an external clock pulse.



DIP-16

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



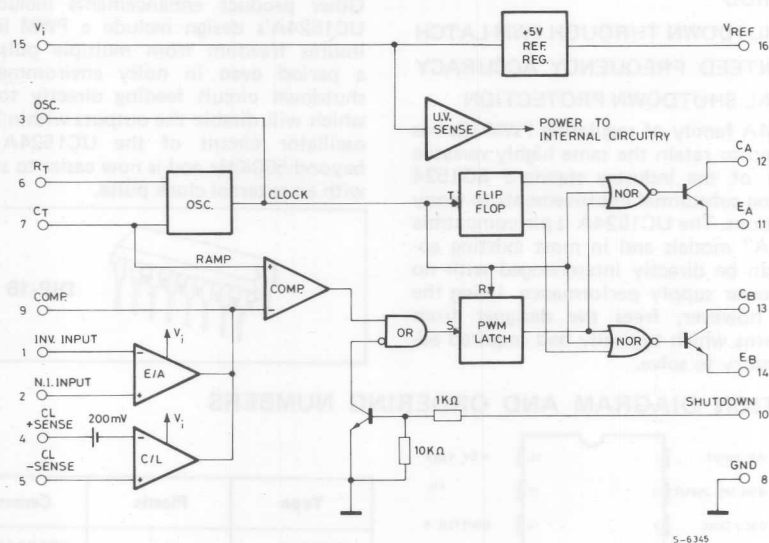
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Type	Plastic	Ceramic
UC1524A	—	UC1524AJ
UC2524A	UC2524AN	UC2524AJ
UC3524A	UC3524AN	UC3524AJ

ABSOLUTE MAXIMUM RATINGS

V_I	Supply voltage	40	V
V_C	Collector supply voltage: UC1524A, UC2524A	60	V
	UC3524A	50	V
I_C	Collector output current (each output)	200	mA
I_R	Reference output current	50	mA
I_T	Current through C_T terminal	-5	mA
P_{tot}	Total power dissipation at $T_{amb} = 70^\circ\text{C}$	1000	mW
T_J	Junction temperature range	-55 to 125	$^\circ\text{C}$
T_{stg}	Storage temperature range	-65 to 150	$^\circ\text{C}$
T_{op}	Operating ambient temperature range UC1524A	-55 to 125	$^\circ\text{C}$
	UC2524A	-25 to 85	$^\circ\text{C}$
	UC3524A	0 to 70	$^\circ\text{C}$

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max.	80	$^{\circ}\text{C/W}$
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UC1524A
UC2524A
UC3524A

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply from $T_{amb} = -55$ to 125°C for the UC1524A, -25 to 85°C for the UC2524A, and 0 to 70°C for the UC3524A; $V_i = V_C = 20\text{V}$)

Parameter	Test conditions	UC1524A UC2524A			UC3524A			Unit		
		Min.	Typ.	Max.	Min.	Typ.	Max.			
TURN-ON CHARACTERISTICS										
V _i	Input voltage	Operating range after Turn-on		8		40	8		40	V
	Turn-on threshold			5.5	7.5	8.5	5.5	7.5	8.5	V
	Turn-on current	V _i = 6V			2.5	4		2.5	4	mA
I _q	Operating current	V _i = 8 to 40V			5	10		5	10	mA
*	Turn-on hysteresis				0.6			0.6		V

REFERENCE SECTION

V_{REF}	Output voltage	$T_j = 25^{\circ}\text{C}$	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line regulation	$V_i = 10$ to 40V		10	20		10	30	mV
ΔV_{REF}	Load regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T^*$	Temperature stability	Over operating range		20	50		20	50	mV
	Short circuit current	$V_{REF} = 0$ $T_j = 25^{\circ}\text{C}$		80	100		80	100	mA
*	Output noise voltage	$10\text{Hz} \leq f \leq 10\text{KHz}$, $T_j = 25^{\circ}\text{C}$		40			40		μV_{rms}
ΔV_{REF}^*	Long term stability	$T_j = 125^{\circ}\text{C}$ 1000Hrs		20	50		20	50	mV

OSCILLATOR SECTION (Unless otherwise specified, $R_T = 2700\Omega$, $C_T = 0.01\mu\text{F}$)

	Initial accuracy	$T_j = 25^{\circ}\text{C}$	41	43	45	39	43	47	KHz
$\Delta f/\Delta T^*$	Temperature stability	Over op. temp. range		1	2		1	2	%
f_{min}	Minimum frequency	$R_T = 150\text{K}\Omega$, $C_T = 0.1\mu\text{F}$			140			120	Hz
f_{max}	Maximum frequency	$R_T = 2\text{K}\Omega$, $C_T = 470\text{pF}$	500			500			KHz
*	Output amplitude	$T_j = 25^{\circ}\text{C}$		3.5			3.5		V
*	Output pulse width	$T_j = 25^{\circ}\text{C}$		0.5			0.5		μs
	Ramp peak		3.3	3.5	3.7	3.3	3.5	3.7	V
	Ramp valley	$T_j = 25^{\circ}\text{C}$	0.7	0.8	0.9	0.7	0.8	0.9	V

ERROR AMPLIFIER SECTION (unless otherwise specified, $V_{CM} = 2.5\text{V}$)

V_{OS}	Input offset voltage			0.5	5		2	10	mV
I_b	Input bias current			1	5		1	10	μA
I_{OS}	Input offset current			0.05	1		0.5	1	μA
CMR	Common mode rejection	$V_{CM} = 1.5$ to 5.5V	60	75		60	75		dB
PSR	Power supply rejection	$V_i = 10$ to 40V	50	60		50	60		dB



UC1524A
UC2524A
UC3524A

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	UC1524A UC2524A			UC3524A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V _O	Output swing	Minimum total range			0.5		5	V
G _v	Open loop voltage gain	$\Delta V_O = 1 \text{ to } 4\text{V}$ $R_L \geq 10\text{M}\Omega$			72	80		dB
B *	Gain-bandwidth	$T_j = 25^\circ\text{C}$ $G_v = 0\text{dB}$			1	3		MHz
	DC Transconduct *†	$T_j = 25^\circ\text{C}$, $30\text{k}\Omega \leq R_L \leq 1\text{M}\Omega$			1.7	2.3		mS

CURRENT LIMIT AMPLIFIER (Unless otherwise specified, pin 5 = 0V)

V _{OS}	Input offset voltage	$T_j = 25^\circ\text{C}$, E/A set for Max. Out.			190	200	210	180	200	220	mV
V _{OS}	Input offset voltage	over op. temp. range			180		220	170		230	mV
I _b	Input bias current					-1	-10		-1	-10	μA
CMR	Common mode rejection	$V_{(\text{pin } 5)} = -0.3 \text{ to } 5.5\text{V}$			50	60		50	60		dB
PSR	Power supply rejection	$V_I = 10 \text{ to } 40\text{V}$			50	60		50	60		dB
V _O	Output swing	Minimum total range			0.5		5	0.5		5	V
G _v	Open loop volt. gain	$\Delta V_O = 1 \text{ to } 4\text{V}$, $R_L \geq 10\text{M}\Omega$			70	80		70	80		dB
t _d *	Delay time	pin 4 to pin 9, $\Delta V_I = 300\text{mV}$				300			300		ns

OUTPUT SECTION (Each output)

V _{CE}	Collector-emitter voltage	$I_C = 100\mu\text{A}$			60	80		50	80		V
I _C	Collector leakage current	$V_{CE} = 50\text{V}$				0.1	20		0.1	20	μA
V _{sat}	Saturation voltage	$I_C = 20\text{mA}$ $I_C = 200\text{mA}$				0.2 1	0.4 2.2		0.2 1	0.4 2.2	V V
V _{EO}	Emitter output voltage	$I_E = 50\text{mA}$			17	18		17	18		V
t _r *	Rise time	$T_j = 25^\circ\text{C}$ $R = 2\text{K}\Omega$				200			200		ns
t _f *	Fall time	$T_j = 25^\circ\text{C}$ $R = 2\text{K}\Omega$				100			100		ns
*	Comparator delay	$T_j = 25^\circ\text{C}$, pin 9 to output				300			300		ns
*	Shutdown delay	$T_j = 25^\circ\text{C}$, pin 10 to output				200			200		ns
	Shutdown threshold	$T_j = 25^\circ\text{C}$ $R_C = 2\text{K}\Omega$			0.5	0.7	1	0.5	0.7	1	V
	Thermal shutdown					165			165		$^\circ\text{C}$

* These parameters are guaranteed by design but not 100% tested in production

† DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation $G_v = g_M R_L$ where R_L is the resistance from pin 9 to ground.

The minimum g_M specification is used to calculate minimum G_v when the error amplifier output is loaded.



UC1524A
UC2524A
UC3524A

Fig. 1 - Supply current vs. input voltage

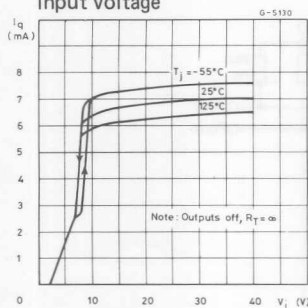


Fig. 2 - Error amplifier voltage gain vs. frequency

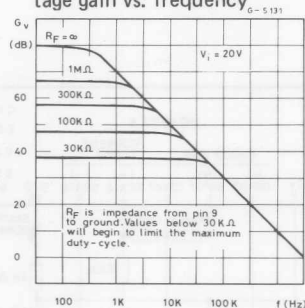


Fig. 3 - PWM duty cycle vs. Vg (one output)

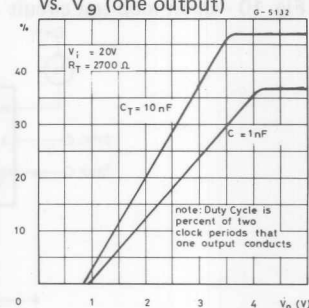


Fig. 4 - Oscillator frequency vs. timing components

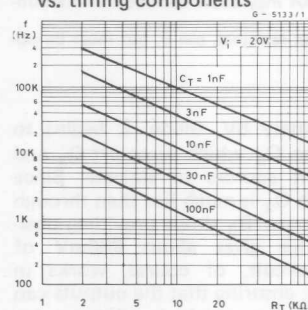


Fig. 5 - Output dead time vs. timing capacitor value

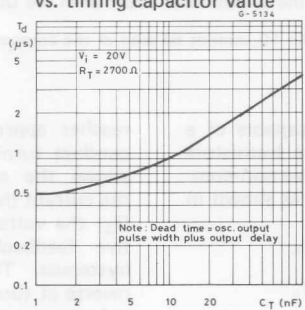


Fig. 6 - Output saturation voltage

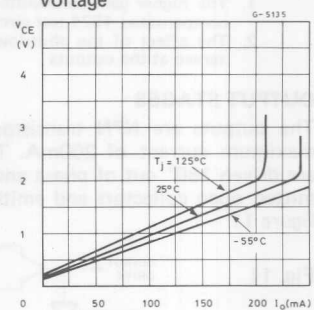


Fig. 7 - Current limit amplifier delay

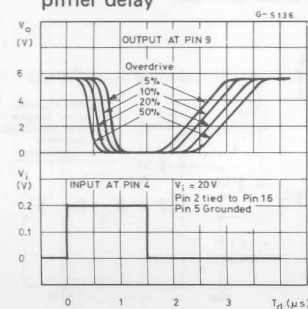


Fig. 8 - Shutdown delay from PWM comparator - pin 9

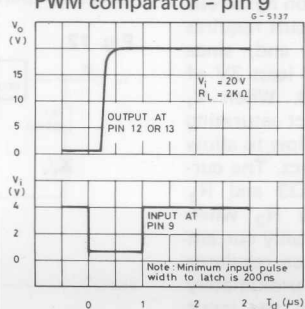
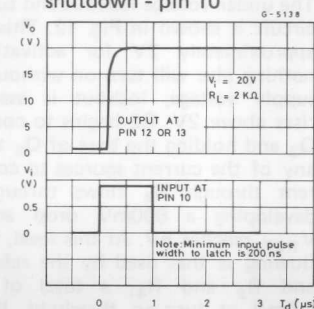


Fig. 9 - Turn-off delay from shutdown - pin 10

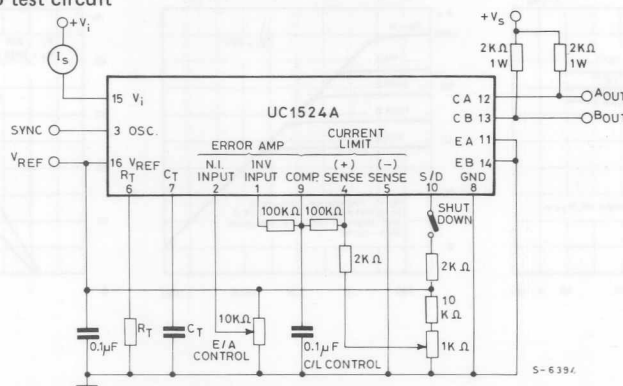




UC1524A
UC2524A
UC3524A

APPLICATION INFORMATION

Fig. 10 - Open-loop test circuit

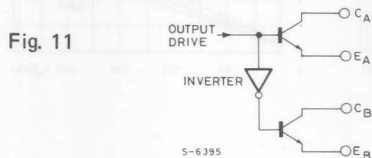


Note: The UC1524A should be able to be tested in any 1524 test circuit with two possible exceptions:

1. The higher gain-bandwidth of the current limit amplifier in the UC1524A may cause oscillations in an uncompensated 1524 test circuit.
2. The effect of the shutdown, pin 10, cannot be seen at the compensation terminal, pin 9, but must be observed at the outputs

OUTPUT STAGES

The outputs are NPN transistors, capable of a maximum current of 200mA. These transistors are driven 180° out of phase and have non-committed open collectors and emitters as shown in figure 11

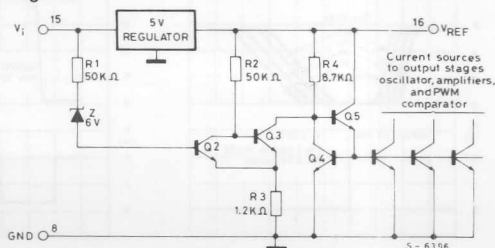


Internal power turn-on circuit

The under-voltage lockout and turn-on hysteresis circuit is shown in Fig. 12. This circuit requires approximately 2V for activation; and, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_i rises above 2V, R2 begins to conduct saturating Q3 and holding the base of Q5 too low to allow any of the current sources to conduct. The current through R4 flows through Q3 and R3 developing a 600mV drop across R3 when V_{REF} reaches 5V. At this level, the only current flowing is that used by the reference regulator and R2 and R4, a total of approximately 2.5mA at turn-on threshold. When the input

reaches approximately 8V, diode, Z begins to conduct turning on Q2 which turns off Q3 and allows the current sources to activate. Since the current through Q2 is much less than through Q3, the voltage across R3 drops providing positive feedback. This gives about 600mV of hysteresis. This circuit, of course, works in reverse at turn off, ensuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 1 shows the relationship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with bootstrapped operation after turn on.

Fig. 12



APPLICATION INFORMATION (continued)

Fig. 13 - Single 5V-10A regulator

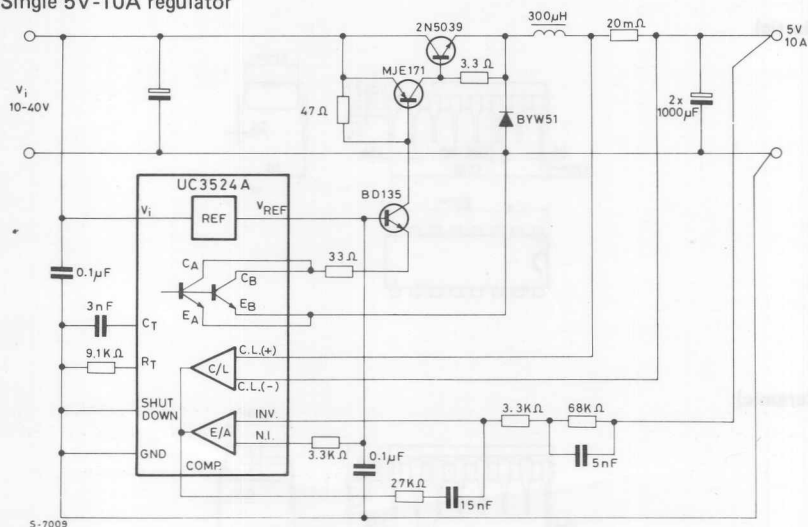
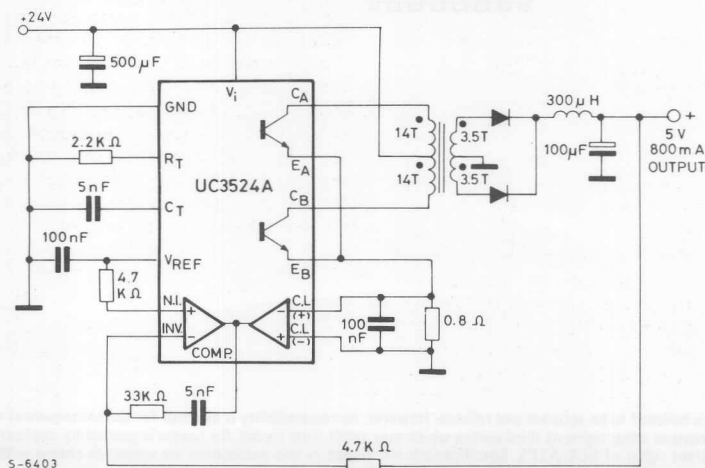


Fig. 14 - 4W DC-DC converter. With higher output voltage and current capability the UC3524A can implement a complete converter with no external transistors.

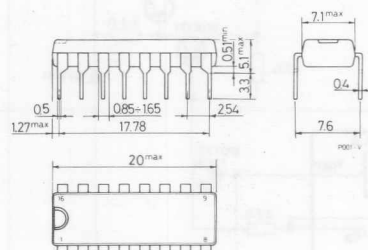




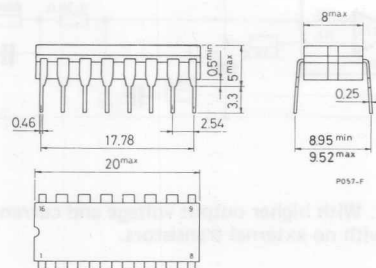
UC1524A
UC2524A
UC3524A

MECHANICAL DATA (Dimensions in mm)

DIP-16 (Plastic)



DIP-16 (Ceramic)



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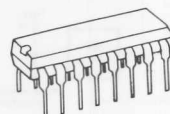
REGULATING PULSE WIDTH MODULATORS

- 8 to 35V OPERATION
- 5.1V REFERENCE TRIMMED TO $\pm 1\%$
- 100Hz to 500KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1V reference is trimmed to $\pm 1\%$ and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry

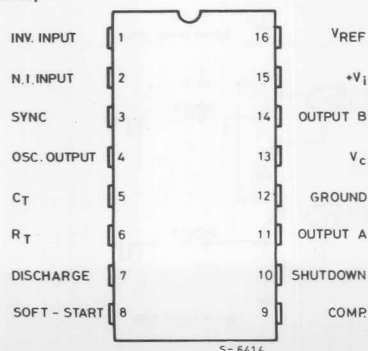
with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period.

The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.



DIP-16

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



Type	Plastic DIP	Ceramic DIP
SG1525A	—	SG1525AJ
SG1527A	—	SG1527AJ
SG2525A	SG2525AN	SG2525AJ
SG2527A	SG2527AN	SG2527AJ
SG3525A	SG3525AN	SG3525AJ
SG3527A	SG3527AN	SG3527AJ



SG1525A/27A
SG2525A/27A
SG3525A/27A

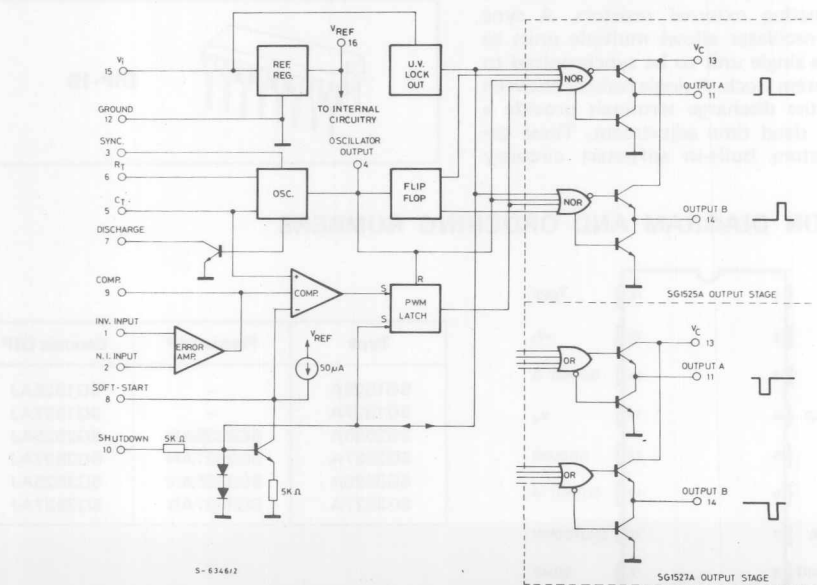
ABSOLUTE MAXIMUM RATINGS

V_i	Supply voltage	40	V
V_c	Collector supply voltage	40	V
I_{osc}	Oscillator charging current	5	mA
I_o	Output current, source or sink	500	mA
I_R	Reference output current	50	mA
I_T	Current through C_T terminal	5	mA
	Logic inputs	-0.3 to + 5.5	V
	Analog inputs	-0.3 to V_i	V
P_{tot}	Total power dissipation at $T_{amb} = 70^\circ\text{C}$	1000	mW
T_j	Junction temperature range	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range	-65 to 150	$^\circ\text{C}$
T_{op}	Operating ambient temperature: SG1525A/27A SG2525A/27A SG3525A/27A	-55 to 125 -25 to 85 0 to 70	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$

THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80 $^\circ\text{C/W}$
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BLOCK DIAGRAM





SG1525A/27A
SG2525A/27A
SG3525A/27A

ELECTRICAL CHARACTERISTICS ($V_I = 20V$, and over operating temperature, unless otherwise specified)

Parameter	Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

REFERENCE SECTION

V_{REF}	Output voltage	$T_J = 25^\circ C$	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line regulation	$V_I = 8 \text{ to } 35V$		10	20		10	20	mV
ΔV_{REF}	Load regulation	$I_L = 0 \text{ to } 20 \text{ mA}$		20	50		20	50	mV
$\Delta V_{REF}/\Delta T^*$	Temp. stability	Over operating range		20	50		20	50	mV
*	Total output variation	Line, load and temperature	5		5.2	4.95		5.25	V
	Short circuit current	$V_{REF} = 0 \quad T_J = 25^\circ C$		80	100		80	100	mA
*	Output noise voltage	$10\text{Hz} \leq f \leq 10\text{kHz}, T_J = 25^\circ C$		40	200		40	200	μV_{rms}
ΔV_{REF}^*	Long term stability	$T_J = 125^\circ C, 1000 \text{ hrs}$		20	50		20	50	mV

OSCILLATOR SECTION**

*, •	Initial accuracy	$T_J = 25^\circ C$		± 2	± 6		± 2	± 6	%
*, •	Voltage stability	$V_I = 8 \text{ to } 35V$		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T^*$	Temp. stability	Over operating range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minim. frequency	$R_T = 200 \text{ K}\Omega \quad C_T = 0.1 \mu F$			120			120	Hz
f_{MAX}	Maxim. frequency	$R_T = 2 \text{ K}\Omega \quad C_T = 470 \text{ pF}$	400			400			KHz
	Current mirror	$I_{RT} = 2 \text{ mA}$	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock amplitude		3	3.5		3	3.5		V
*, •	Clock width	$T_J = 25^\circ C$	0.3	0.5	1	0.3	0.5	1	μs
	Sync threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync input current	Sync voltage = 3.5V		1	2.5		1	2.5	mA

ERROR AMPLIFIER SECTION ($V_{CM} = 5.1V$)

V_{OS}	Input offset voltage		0.5	5		2	10	mV
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SG1525A/27A
SG2525A/27A
SG3525A/27A

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_B Input bias current			1	10		1	10	μA
I_{OS} Input offset current				1			1	μA
DC open loop gain	$R_L \geq 10 M\Omega$	60	75		60	75		dB
* Gain bandwidth product	$G_V = 0 \text{ dB}$ $T_J = 25^\circ C$	1	2		1	2		MHz
* DC transconduct.	$30 K\Omega \leq R_L \leq 1 M\Omega$ $T_J = 25^\circ C$	1.1	1.5		1.1	1.5		mS
Output low level			0.2	0.5		0.2	0.5	V
Output high level		3.8	5.6		3.8	5.6		V
CMR Comm. mode rejec.	$V_{CM} = 1.5 \text{ to } 5.2V$	60	75		60	75		dB
PSR Supply voltage rejection	$V_I = 8 \text{ to } 35V$	50	60		50	60		dB

PWM COMPARATOR

Minim. duty-cycle				0			0	%
Maxim. duty-cycle		45	49		45	49		%
* Input threshold	Zero duty-cycle	0.7	0.9		0.7	0.9		V
	Maximum duty-cycle		3.3	3.6		3.3	3.6	V
* Input bias current			0.05	1		0.05	1	μA

SHUTDOWN SECTION

Soft start current	$V_{SD} = 0V$, $V_{SS} = 0V$	25	50	80	25	50	80	μA
Soft start low level	$V_{SD} = 2.5V$		0.4	0.7		0.4	0.7	V
Shutdown threshold	To outputs, $V_{SS} = 5.1V$ $T_J = 25^\circ C$	0.6	0.8	1	0.6	0.8	1	V
Shutdown input current	$V_{SD} = 2.5V$		0.4	1		0.4	1	mA
* Shutdown delay	$V_{SD} = 2.5V$ $T_J = 25^\circ C$		0.2	0.5		0.2	0.5	μs



SG1525A/27A
SG2525A/27A
SG3525A/27A

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

OUTPUT DRIVERS (Each output) ($V_C = 20V$)

Output low level	$I_{\text{sink}} = 20 \text{ mA}$		0.2	0.4		0.2	0.4	V
	$I_{\text{sink}} = 100 \text{ mA}$		1	2		1	2	V
Output high level	$I_{\text{source}} = 20 \text{ mA}$	18	19		18	19		V
	$I_{\text{source}} = 100 \text{ mA}$	17	18		17	18		V
Under-voltage lockout	V_{comp} and $V_{\text{SS}} = \text{high}$	6	7	8	6	7	8	V
I_C Collector leakage	$V_C = 35V$			200			200	μA
t_r^* Rise time	$C_L = 1 \text{ nF}$, $T_J = 25^\circ\text{C}$		100	600		100	600	ns
t_f^* Fall time	$C_L = 1 \text{ nF}$, $T_J = 25^\circ\text{C}$		50	300		50	300	ns

TOTAL STANDBY CURRENT

I_S Supply current	$V_I = 35V$		14	20		14	20	mA
----------------------	-------------	--	----	----	--	----	----	----

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

- Tested at $f_{\text{osc}} = 40 \text{ KHz}$ ($R_T = 3.6 \text{ K}\Omega$, $C_T = 0.1 \text{ }\mu\text{F}$, $R_D = 0\Omega$). Approximate oscillator frequency is defined by:

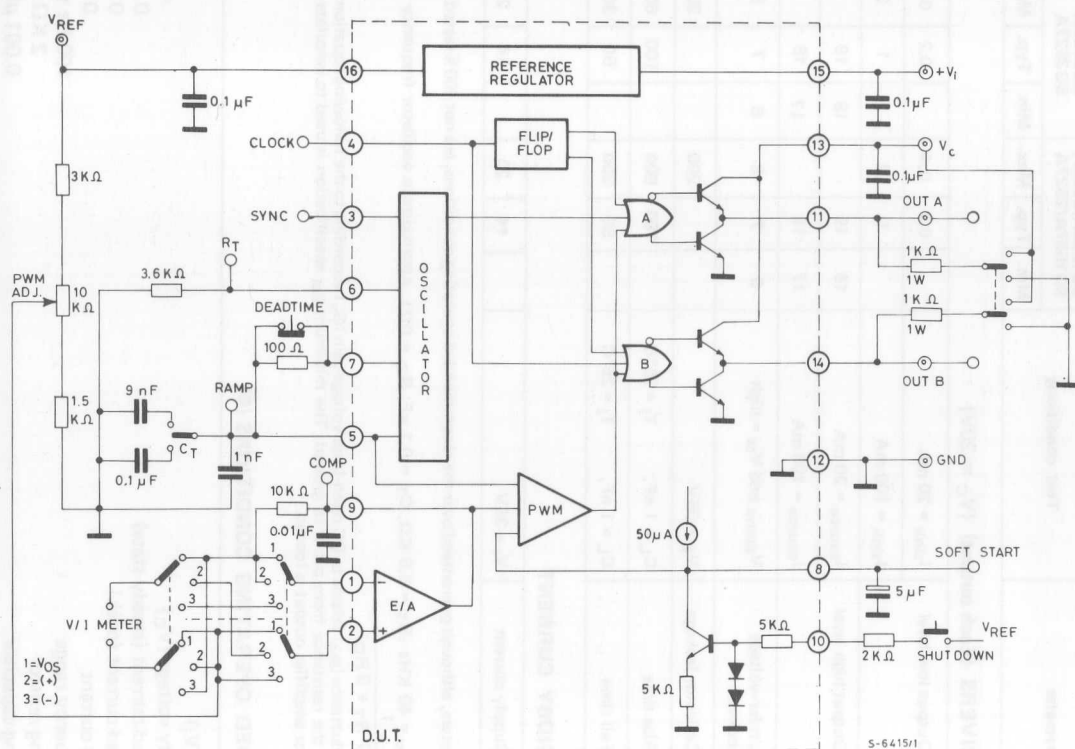
$$f = \frac{1}{C_T (0.7 R_T + 3 R_D)}$$

- DC transconductance (g_M) relates to DC open-loop voltage gain (G_V) according to the following equation: $G_V = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_V when the error amplifier output is loaded.

RECOMMENDED OPERATING CONDITIONS (●)

Input voltage (V_I)	8 to 35 V
Collector supply voltage (V_C)	4.5 to 35 V
Sink/source load current (steady state)	0 to 100 mA
Sink/source load current (peak)	0 to 400 mA
Reference load current	0 to 20 mA
Oscillator frequency range	100 Hz to 400 KHz
Oscillator timing resistor	2 K Ω to 150 K Ω
Oscillator timing capacitor	0.001 μF to 0.1 μF
Dead time resistor range	0 to 500 Ω

(●) Range over which the device is functional and parameter limits are guaranteed.



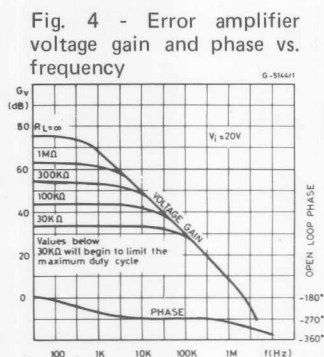
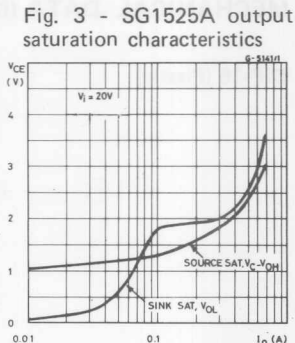
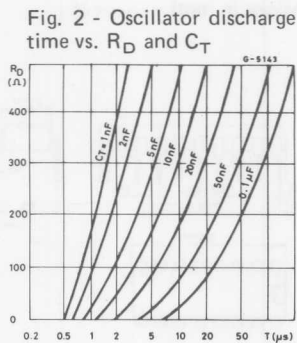
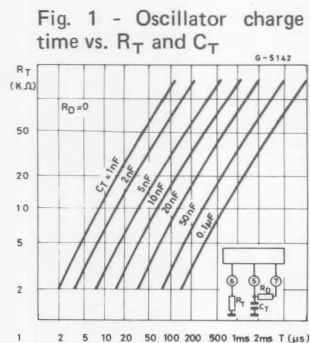
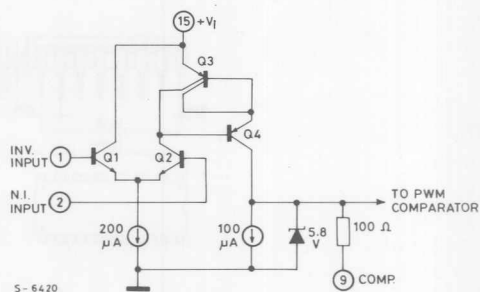


Fig. 5 - SG1525A error amplifier



PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μ A to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is

immediately set providing the fastest turn-off signal to the outputs; and a 150 μ A current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

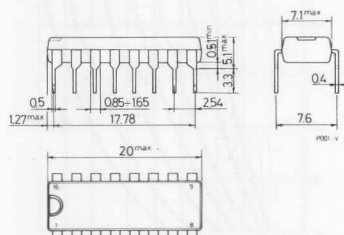
Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.



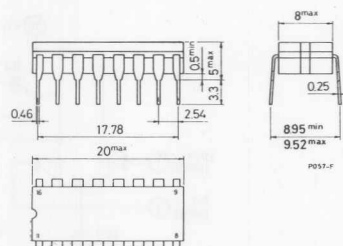
SG1525A/27A
SG2525A/27A
SG3525A/27A

MECHANICAL DATA (Dimensions in mm)

DIP-16 (Plastic)



DIP-16 (Ceramic)



PAGE OUT OF
SEQUENCE

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SG1525A/27A
SG2525A/27A
SG3525A/27A

Fig. 6 - SG1525A oscillator schematic

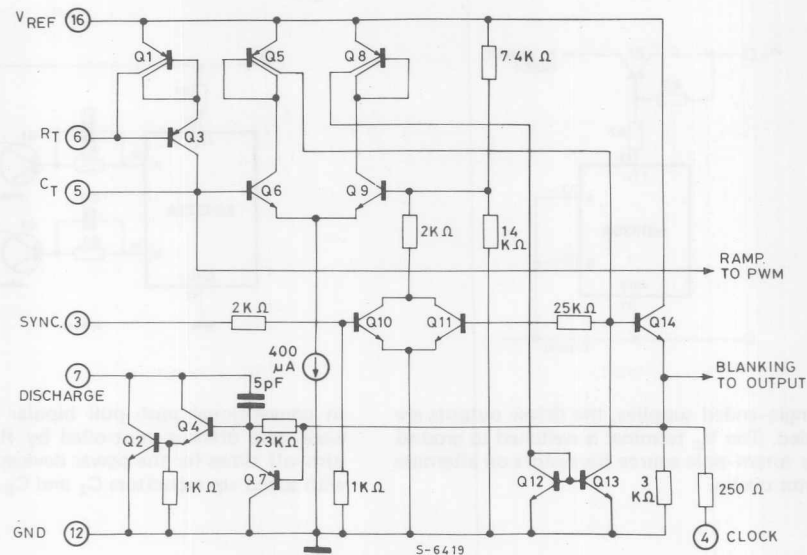


Fig. 7 - SG1525A output circuit (½ circuit shown)

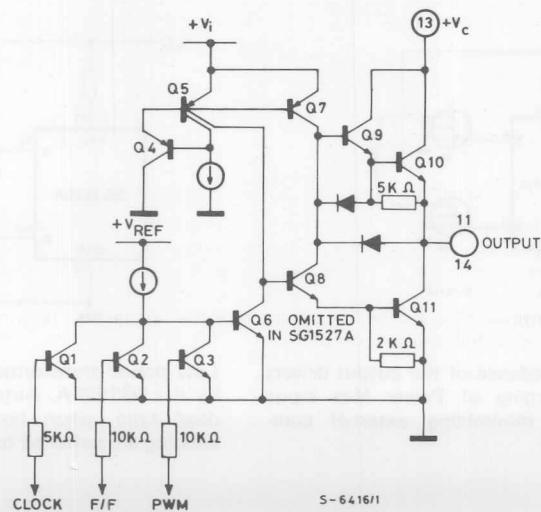
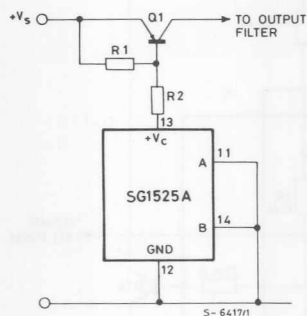
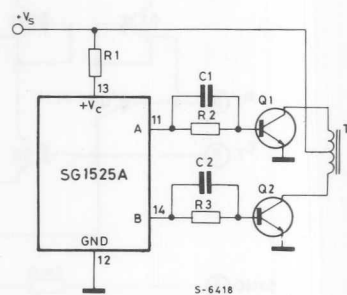


Fig. 7



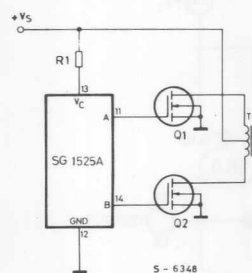
For single-ended supplies, the driver outputs are grounded. The V_c terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Fig. 8



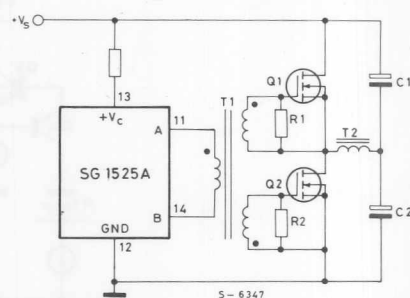
In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3 . Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2 .

Fig. 9



The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Fig. 10



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

HIGH CURRENT SWITCHING REGULATOR

- 4A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 100% DUTY CYCLE RANGE
- PRECISE ($\pm 2\%$) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200 KHz
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONOUS PWM
- THERMAL SHUTDOWN

The L296 is a stepdown power switching regulator delivering 4A at a voltage variable from 5.1V to 40V.

Features of the device include programmable

current limiting, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296 is mounted in a 15-lead Multiwatt[®] plastic power package and requires very few external components.

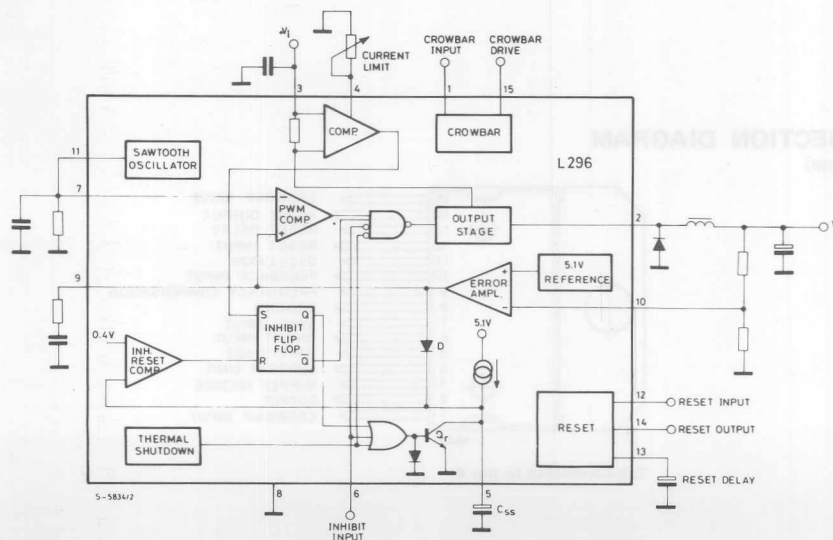
Efficient operation at switching frequencies up to 200kHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.



**Multiwatt[®]
(15-lead)**

ORDERING NUMBER: L296

BLOCK DIAGRAM





L296

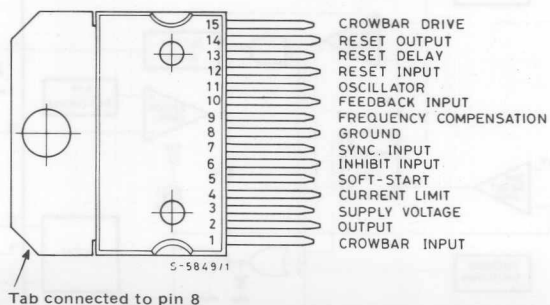


ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (pin 3)	50	V
$V_i - V_2$	Input to output voltage difference	50	V
V_2	Output DC voltage	-1	V
	Output peak voltage at $t = 0.1 \mu\text{sec}$ $f = 200 \text{ kHz}$	-7	V
V_1, V_{12}	Voltage at pins 1, 12	10	V
V_6, V_{15}	Voltage at pins 6, and 15	15	V
V_4, V_5, V_7, V_9	Voltage at pins 4, 5, 7 and 9	5.5	V
V_{10}, V_6	Voltage at pins 10 and 6	7	V
V_{14}	Voltage at pin 14 ($I_{14} \leq 1 \text{ mA}$)	V_i	
I_9	Pin 9 sink current	1	mA
I_{11}	Pin 11 source current	20	mA
I_{14}	Pin 14 sink current ($V_{14} < 5\text{V}$)	50	mA
P_{tot}	Power dissipation at $T_{\text{case}} \leq 90^\circ\text{C}$	20	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	$^\circ\text{C}$

THERMAL DATA

$R_{\text{th j-case}}$	Thermal resistance junction-case	max	3 $^\circ\text{C/W}$
$R_{\text{th j-amb}}$	Thermal resistance junction-ambient	max	35 $^\circ\text{C/W}$

CONNECTION DIAGRAM
(top view)

**L296****PIN FUNCTIONS**

N°	NAME	FUNCTION
1	CROWBAR INPUT	Voltage sense input for crowbar overvoltage protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator output.
3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the L296's internal logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL — level remote inhibit. A logic high level on this input disables the L296.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common ground terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.

**L296****PIN FUNCTIONS** (continued)

N°	NAME	FUNCTION
12	RESET INPUT	Input of the reset circuit. The threshold is roughly 5V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION(refer to the block diagram)

The L296 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to $\pm 2\%$). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator

resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The crowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

CIRCUIT OPERATION (continued)

Fig. 1 - Reset output waveforms

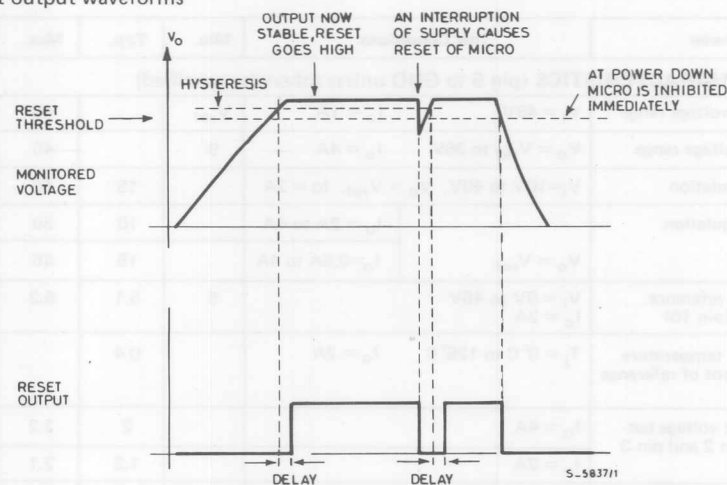


Fig. 2 - Soft start waveforms

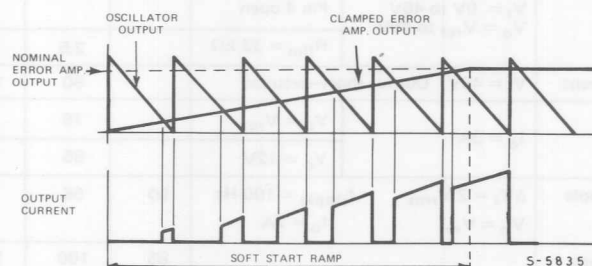
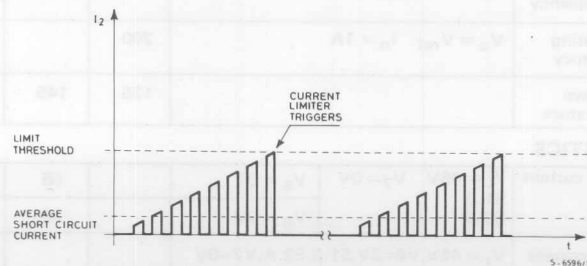


Fig. 3 - Current limiter waveforms





L296

ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_j = 25^\circ\text{C}$, $V_i = 35\text{V}$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)						
V_o Output voltage range	$V_i = 46\text{V}$ $I_o = 1\text{A}$	V_{ref}		40	V	4
V_i Input voltage range	$V_o = V_{ref}$ to 36V $I_o = 4\text{A}$	9		46	V	4
ΔV_o Line regulation	$V_i = 10\text{V}$ to 40V , $V_o = V_{ref}$, $I_o = 2\text{A}$		15	50	mV	4
ΔV_o Load regulation	$V_o = V_{ref}$	$I_o = 2\text{A}$ to 4A	10	30	mV	4
		$I_o = 0.5\text{A}$ to 4A	15	45	mV	4
V_{ref} Internal reference voltage (pin 10)	$V_i = 9\text{V}$ to 46V $I_o = 2\text{A}$	5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$ Average temperature coefficient of reference voltage	$T_j = 0^\circ\text{C}$ to 125°C $I_o = 2\text{A}$		0.4		mV/ $^\circ\text{C}$	
V_d Dropout voltage between pin 2 and pin 3	$I_o = 4\text{A}$		2	3.2	V	4
	$I_o = 2\text{A}$		1.3	2.1	V	4
I_{om} Maximum operating load current	$V_i = 9\text{V}$ to 46V , $V_o = V_{ref}$ to 36V	4			A	4
I_{2L} Current limiting threshold (pin 2)	$V_i = 9\text{V}$ to 46V $V_o = V_{ref}$ to 40V	Pin 4 open		8	A	4
		$R_{lim} = 33\text{ k}\Omega$	2.5		A	4
I_{SH} Input average current	$V_i = 46\text{V}$; Output short-circuited		60	100	mA	4
η Efficiency	$I_o = 3\text{A}$	$V_o = V_{ref}$	75		%	4
		$V_o = 12\text{V}$	85		%	4
SVR Supply voltage ripple rejection	$\Delta V_i = 2 V_{rms}$ $f_{ripple} = 100\text{ Hz}$ $V_o = V_{ref}$ $I_o = 2\text{A}$	50	56		dB	4
f Switching frequency		85	100	115	kHz	4
$\frac{\Delta f}{\Delta V_i}$ Voltage stability of switching frequency	$V_i = 9\text{V}$ to 46V		0.5		%	4
$\frac{\Delta f}{\Delta T_j}$ Temperature stability of switching frequency	$T_j = 0^\circ\text{C}$ to 125°C		1		%	4
f_{max} Maximum operating switching frequency	$V_o = V_{ref}$ $I_o = 1\text{A}$	200			kHz	—
T_{sd} Thermal shutdown junction temperature		135	145		$^\circ\text{C}$	—

DC CHARACTERISTICS

I_{3Q} Quiescent drain current	$V_i = 46\text{V}$ $V_7 = 0\text{V}$	$V_6 = 0\text{V}$		66	85	mA	6a
	S1:B S2:B	$V_6 = 3\text{V}$		30	40	mA	6a
$-I_{2L}$ Output leakage current	$V_i = 46\text{V}$, $V_6 = 3\text{V}$, S1:B, S2:A, $V_7 = 0\text{V}$				2	mA	6a

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
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SOFT START

I_{5so} Source current	$V_6 = 0V, V_5 = 3V$	100	130	160	μA	6b
I_{5si} Sink current	$V_6 = 3V, V_5 = 3V$	50	70	120	μA	6b

INHIBIT

V_{6L} Low input voltage	$V_1 = 9V$ to 46V	$S1 : B$ $S2 : B$	-0.3		0.8	V	6a
V_{6H} High input voltage	$V_7 = 0V$		2		5.5	V	6a
$-I_{6L}$ Input current with low input voltage	$V_1 = 9V$ to 46V	$V_6 = 0.8V$			10	μA	6a
$-I_{6H}$ Input current with high input voltage	$V_7 = 0V$ $S1 : B$ $S2 : B$	$V_6 = 2V$			3	μA	6a

ERROR AMPLIFIER

V_{9H} High level output voltage	$V_{10} = 4.7V, I_9 = 100\mu A, S1 : A, S2 : A$	3.5			V	6c
V_{9L} Low level output volt.	$V_{10} = 5.3V, I_9 = 100\mu A, S1 : A, S2 : E$			0.5	V	6c
I_{9si} Sink output current	$V_{10} = 5.3V, S1 : A, S2 : B$	100	150		μA	6c
$-I_{9so}$ Source output current	$V_{10} = 4.7V, S1 : A, S2 : D$	100	150		μA	6c
I_{10} Input bias current	$V_{10} = 5.2V, S1 : B$		2	10	μA	6c
G_v DC open loop Gain	$V_9 = 1V$ to 3V, $S1 : A, S2 : C$	46	55		dB	6c

OSCILLATOR AND PWM COMPARATOR

$-I_7$ Input bias current of PWM comparator	$V_7 = 0.5V$ to 3.5V			5	μA	6a
$-I_{11}$ Oscillator source current	$V_{11} = 2V, S1 : A, S2 : B$	5			mA	6a

RESET

V _{12R} Rising threshold voltage	V _i = 9V to 46V, S1 : B S2 : B		V _{ref} -150mV	V _{ref} -100mV	V _{ref} -50mV	V	6d
V _{12F} Falling threshold voltage			4.75	V _{ref} -150mV	V _{ref} -100mV	V	6d
V _{13D} Delay threshold voltage	V ₁₂ = 5.3V, S1 : A S2 : B		4.3	4.5	4.7	V	6d
V _{13H} Delay threshold voltage hysteresis				100		mV	6d
V _{14S} Output saturation volt.	I ₁₄ = 16mA; V ₁₂ =4.7V; S1, S2 : B				0.4	V	6d
I ₁₂ Input bias current	V ₁₂ = 0V to V _{ref} , S1 : B, S2 : B			1	3	μA	6d
-I _{13 so} Delay source current	V ₁₃ = 3V S1 : A	V ₁₂ = 5.3V	70	110	140	μA	6d
I _{13 si} Delay sink current	S2 : B	V ₁₂ = 4.7V	10			mA	6d
I ₁₄ Output leakage current	V _i = 46V, V ₁₂ =5.3V, S1 :B, S2 :A				100	μA	6d

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
CROWBAR						
V ₁	Input threshold voltage S1 : B	5.5	6	6.4	V	6b
V ₁₅	Output saturation voltage V _i = 9V to 46V, I ₁₅ = 5mA V ₁ = 5.4V S1 : A		0.2	0.4	V	6b
I ₁	Input bias current V ₁ = 6V, S1 : B			10	μA	6b
-I ₁₅	Output source current V _i = 9V to 46V, V ₁₅ = 2V V ₁ = 6.5V S1 : B	70	100		mA	6b

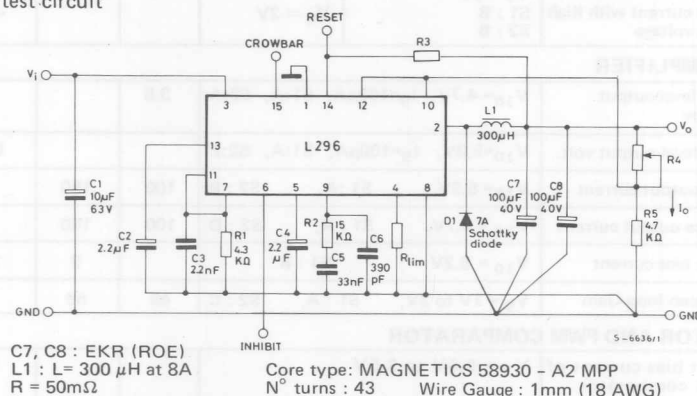
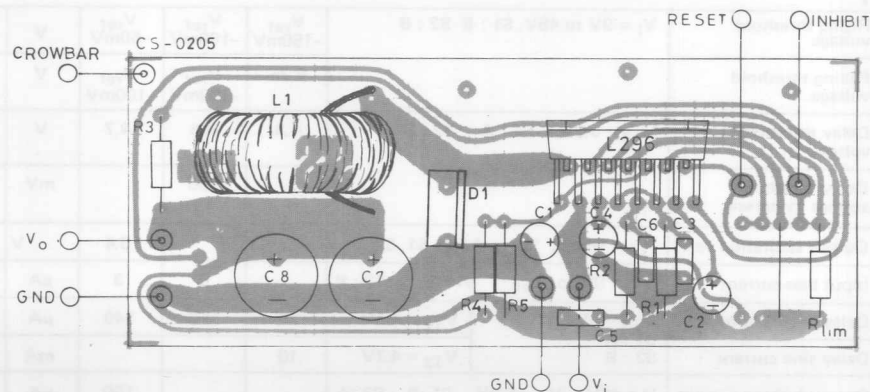
Fig. 4 - Dynamic test circuit

Fig. 5 - PC. board and component layout of the circuit of fig. 4 (1:1 scale)


Fig. 6 – DC test circuits

Fig. 6a

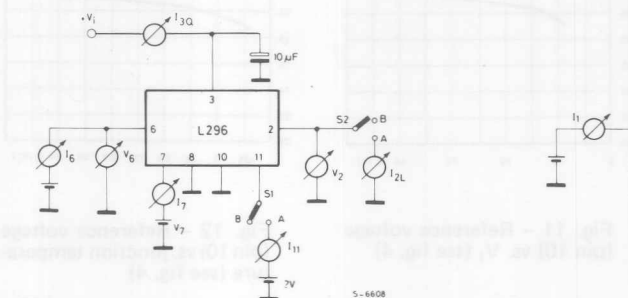


Fig. 6b

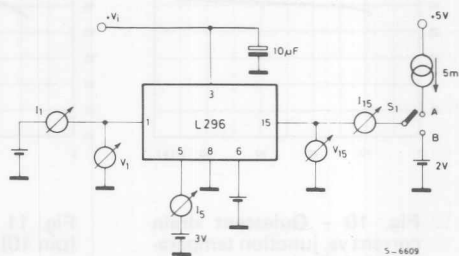
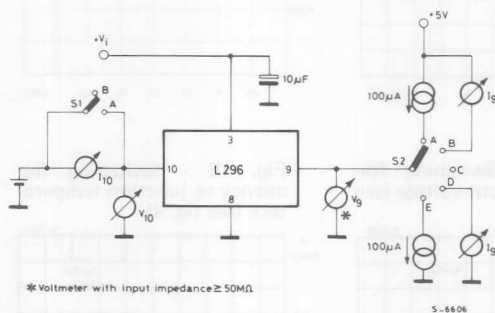


Fig. 6c



- 1 - Set V_{10} for $V_9 = 1V$
- 2 - Change V_{10} to obtain $V_9 = 3V$
- 3 - $G_v = \frac{\Delta V_9}{\Delta V_{10}} = \frac{2V}{\Delta V_{10}}$

Fig. 6d

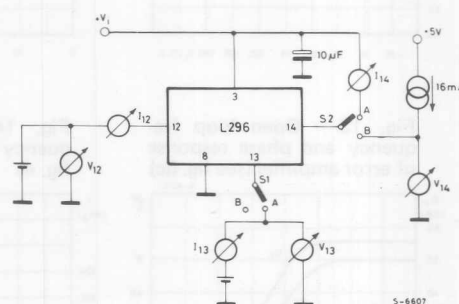


Fig. 7 - Quiescent drain current vs. supply voltage (0% duty cycle - see fig. 6a)

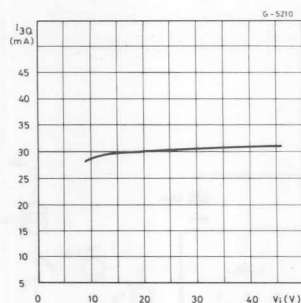


Fig. 8 - Quiescent drain current vs. supply voltage (100% duty cycle see fig. 6a)

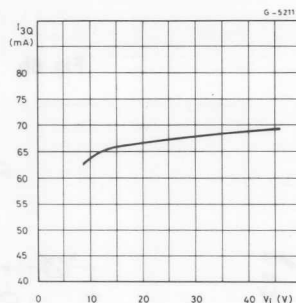


Fig. 9 - Quiescent drain current vs. junction temperature (0% duty cycle - see fig. 6a)

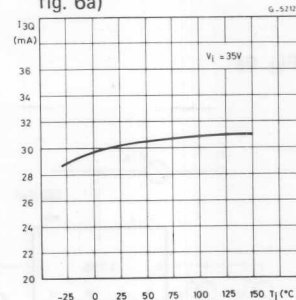


Fig. 10 - Quiescent drain current vs. junction temperature (100% duty cycle - see fig. 6a)

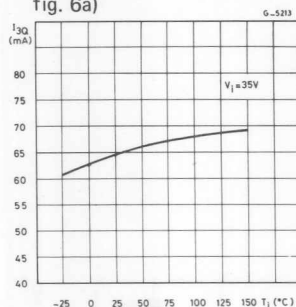


Fig. 11 - Reference voltage (pin 10) vs. V_i (see fig. 4)

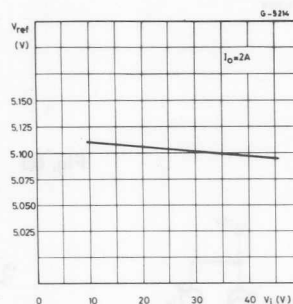


Fig. 12 - Reference voltage (pin 10) vs. junction temperature (see fig. 4)

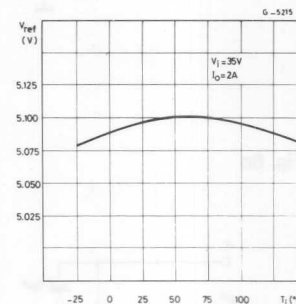


Fig. 13 - Open loop frequency and phase response of error amplifier (see fig. 6c)

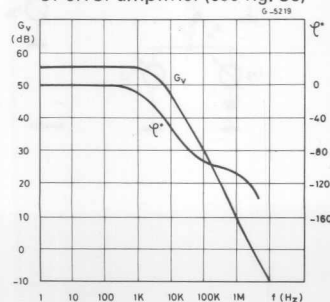


Fig. 14 - Switching frequency vs. input voltage (see fig. 4)

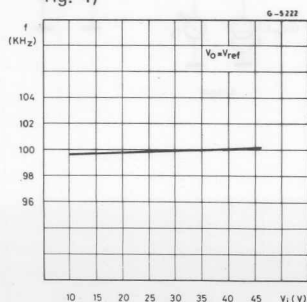


Fig. 15 - Switching frequency vs. junction temperature (see fig. 4)

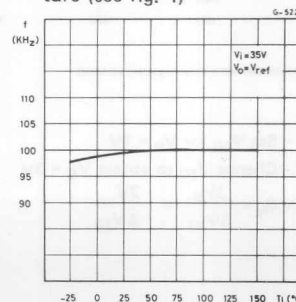


Fig. 16 - Switching frequency vs. R_1 (see fig. 4)

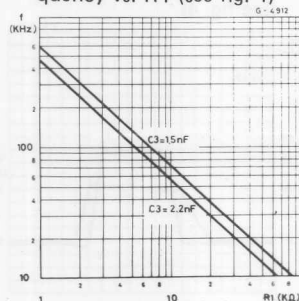


Fig. 17 - Line transient response (see fig. 4)

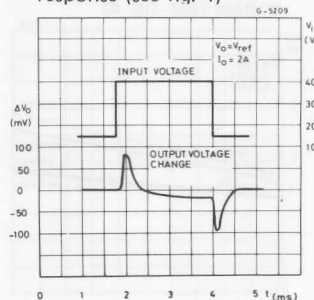


Fig. 18 - Load transient response (see fig. 4)

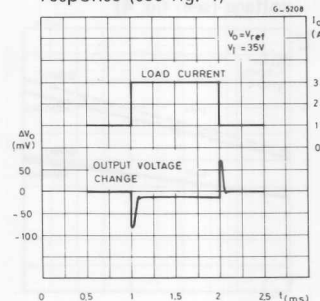


Fig. 19 - Supply voltage ripple rejection vs. frequency (see fig. 4)

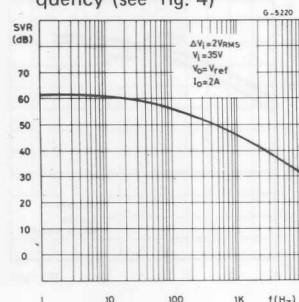


Fig. 20 - Dropout voltage between pin 3 and pin 2 vs. current at pin 2

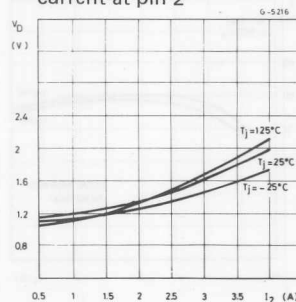


Fig. 21 - Dropout voltage between pin 3 and pin 2 vs. junction temperature

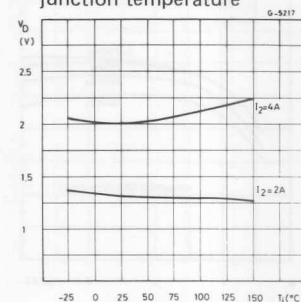


Fig. 22 - Power dissipation derating curve

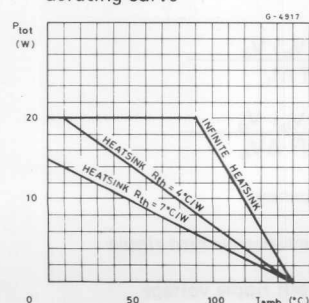


Fig. 23 - Power dissipation (L296 only) vs. input voltage

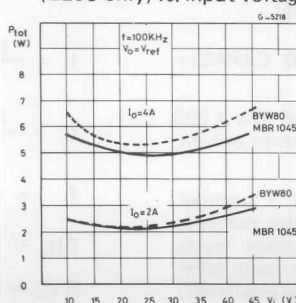
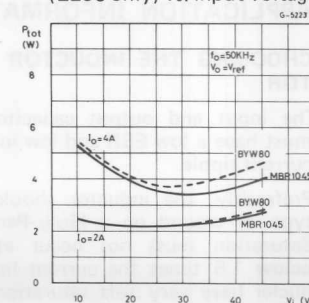


Fig. 24 - Power dissipation (L296 only) vs. input voltage





L296

Fig. 25 - Power dissipation (L296 only) vs. output voltage (see fig. 4)

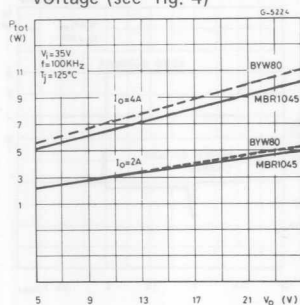


Fig. 26 - Power dissipation (L296 only) vs. output voltage (see fig. 4)

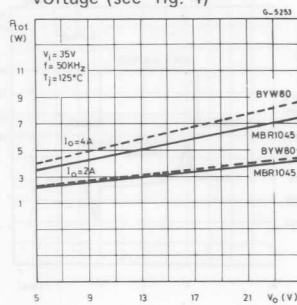


Fig. 27 - Voltage and current waveforms at pin 2 (see fig. 4)

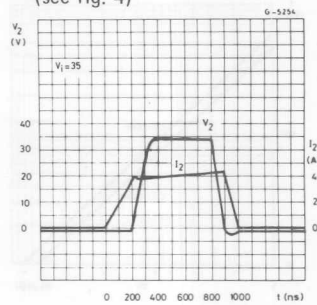


Fig. 28 - Efficiency vs. output current

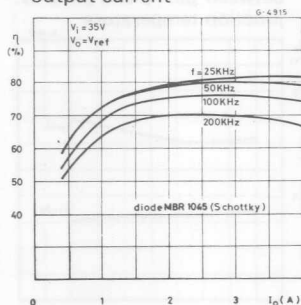


Fig. 29 - Efficiency vs. output current

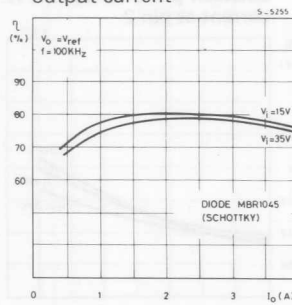
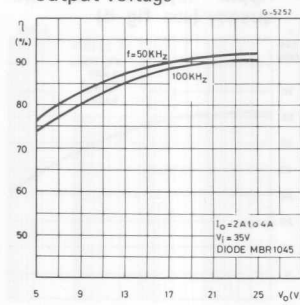


Fig. 30 - Efficiency vs. output voltage



APPLICATION INFORMATION

CHOOSING THE INDUCTOR AND CAPACITOR

The input and output capacitors of the L296 must have a low ESR and low inductance at high current ripple.

Preferably, the inductor should be a toroidal type or wound on a Moly-Permalloy nucleus. Saturation must not occur at current levels below 1.5 times the current limiter level. MPP nuclei have very soft saturation characteristics.

$$L = \frac{(V_i - V_o) V_o}{V_i f \Delta I_L}$$

$$C = \frac{(V_i - V_o) V_o}{8L f^2 \Delta V_o}$$

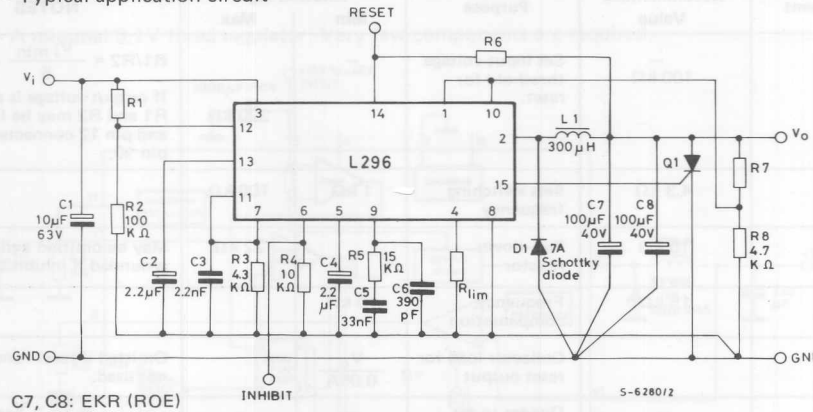
f = frequency

ΔI_L = Inductance current ripple

ΔV_o = Output ripple voltage

APPLICATION INFORMATION

Fig. 31 - Typical application circuit

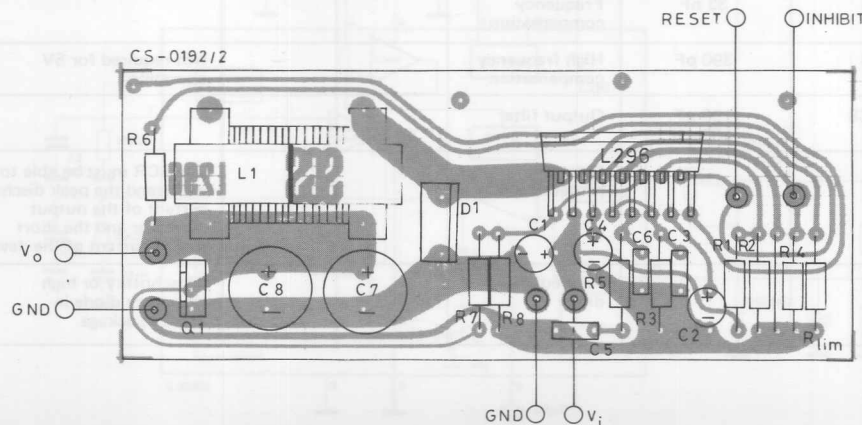


SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	—
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633& - G0500 - X127)	40	2 x 0.8 mm.	—
VOGT 250 µH Toroidal coil, part number 5730501800			

Resistor values for standard output voltages		
Vo	R8	R7
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

Fig. 32 - P.C. board and component layout of the circuit of fig. 31 (1 : 1 scale)



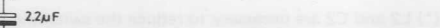


L296

SELECTION OF COMPONENT VALUES (See fig. 31)

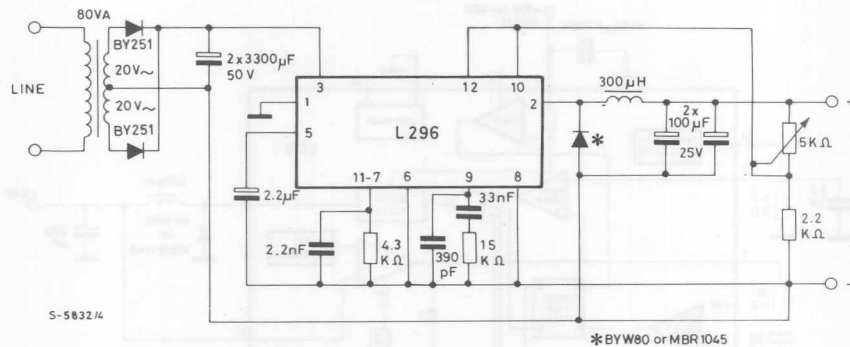
Component	Recommended Value	Purpose	Allowed range		NOTES
			Min	Max	
R1 R2	— 100 k Ω	Set input voltage threshold for reset.	—	220 k Ω	$R1/R2 = \frac{V_{i \min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 k Ω	Sets switching frequency	1 k Ω	100 k Ω	
R4	10 k Ω	Pull-down resistor		22 k Ω	May be omitted and pin 6 grounded if inhibit not used.
R5	15 k Ω	Frequency compensation	10 k Ω		
R6		Collector load for reset output	$\frac{V_o}{0.05A}$		Omitted if reset function not used.
R7 R8	— 4.7 k Ω	Divider to set output voltage	— —	— 10 k Ω	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}} -$
R _{lim}	—	Sets current limit level			If R _{lim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 μ F	Stability	1 μ F		
C2	2.2 μ F	Sets reset delay	—	—	Omitted if reset function not used.
C3	2.2 nF	Sets switching frequency	1 nF	3.3 nF	
C4	2.2 μ F	Soft start	1 μ F	—	Also determines average short circuit current.
C5	33 nF	Frequency compensation			
C6	390 pF	High frequency compensation	—	—	Not required for 5V operation
C7,C8 L1	100 μ F 300 μ H	Output filter			
Q1		Crowbar protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation diode			7A schottky or high efficiency diode in D0220 package

are required.



APPLICATION INFORMATION (continued)

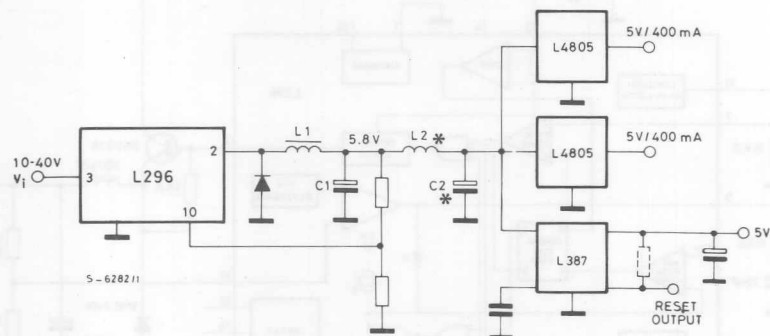
Fig. 35 - Programmable power supply

 $V_o = 5.1 \text{ to } 15\text{V}$
$$I_o = 4A \text{ max. (min. load current} = 100 \text{ mA)}$$
 $\text{ripple} \leq 20 \text{ mV}$

load regulation (1A to 4A) = 10 mV ($V_o = 5.1\text{V}$)

line regulation ($220V \pm 15\%$ and to $I_o = 3A$) = 15 mV ($V_o = 5.1V$)

Fig. 36 – Preregulator for distributed supplies.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

APPLICATION INFORMATION (continued)

Fig. 37 - In multiple supplies several L296s can be synchronized as shown.

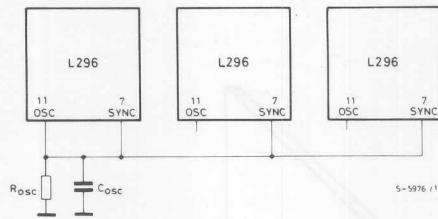


Fig. 38 - Voltage sensing for remote load

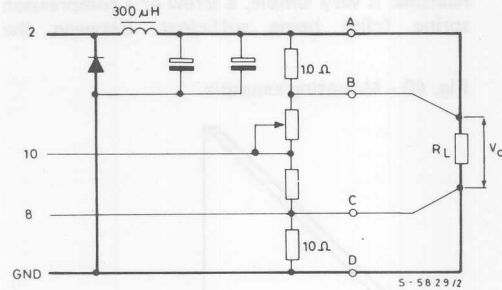
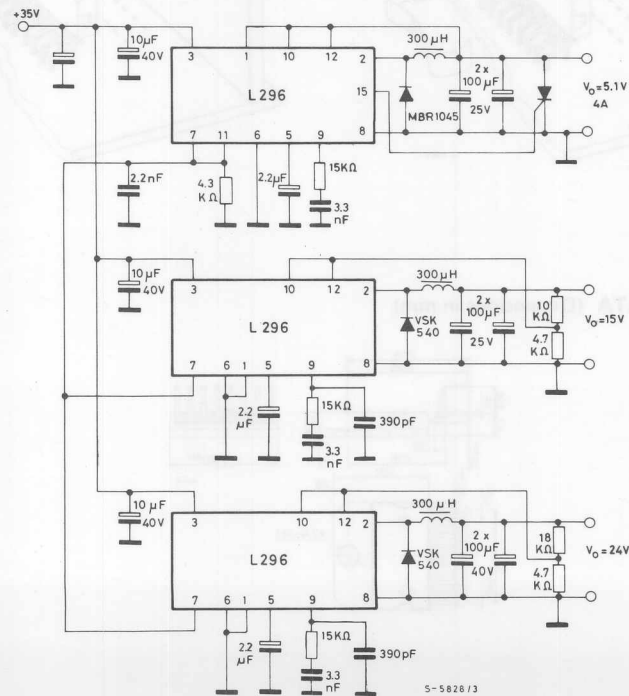


Fig. 39 - A 5.1V/15V/24V multiple supply. Note the synchronization of the three L296s.

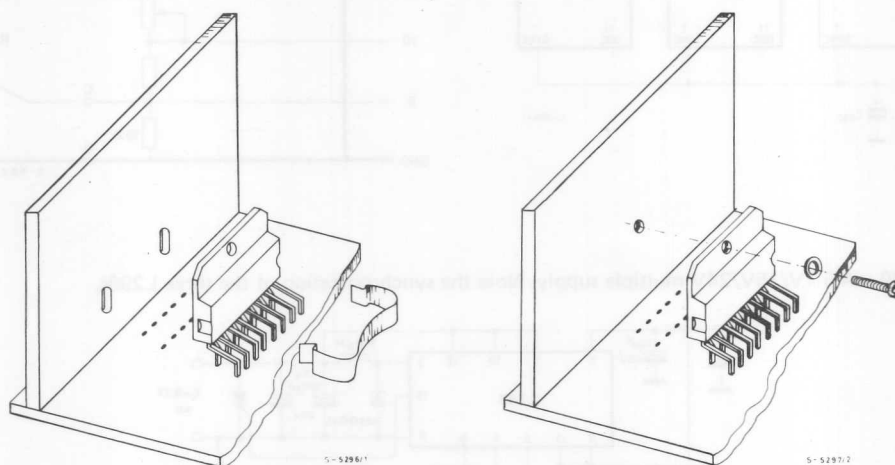


MOUNTING INSTRUCTIONS

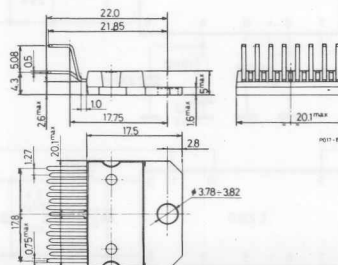
The power dissipated in the circuit must be removed by adding an external heatsink. Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the

heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 40 - Mounting example



MECHANICAL DATA (Dimensions in mm)





TECHNICAL NOTE 165

DESIGNING WITH THE L296 MONOLITHIC POWER SWITCHING REGULATOR

by G. Gattavari

A cost-effective replacement for costly hybrids, the SGS L296 Power Switching Regulator delivers 4A at an output voltage of 5.1V to 40V and includes many popular supply features. This comprehensive application guide explains how the device operates and how it is used. Typical application circuits are also presented.

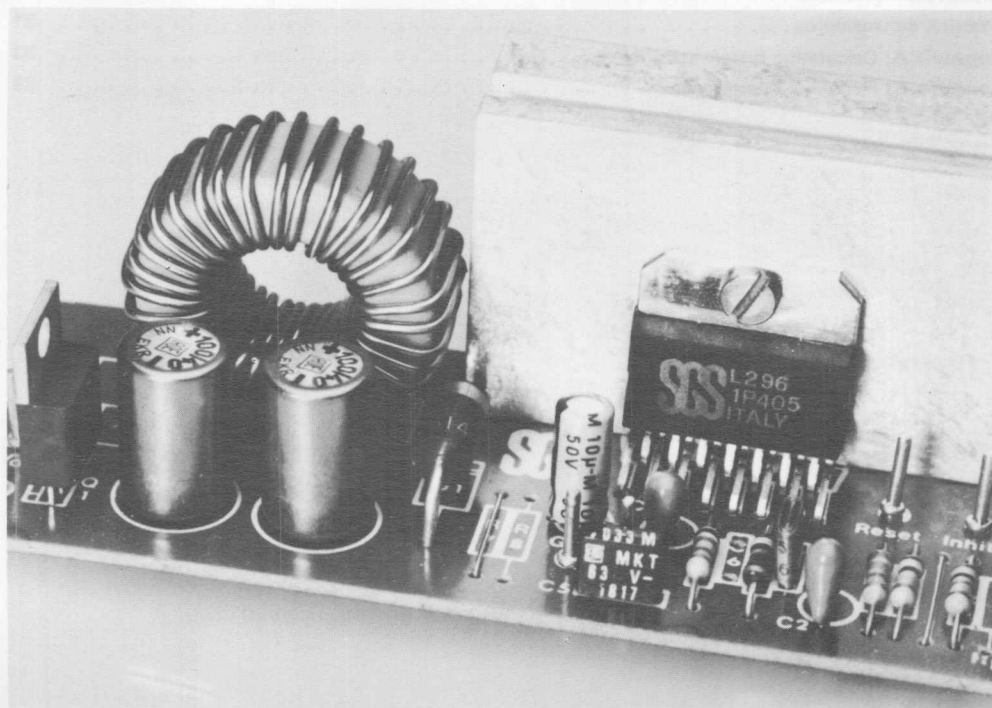


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The SGS L296 is the first monolithic switching regulator in plastic package which includes the power section. Moreover, the circuit includes all the functions which make it specially suited for microprocessor supply.

Before the introduction of L296, which realizes the step down configuration, this function was implemented with discrete power components driven by integrated PWM regulator circuits (giving a maximum output current of 300 to 400 mA) or with hybrid circuits. Both of these solutions are characterized by a low efficiency of the power transistor. For this reason it is generally necessary to operate at frequencies in the 20kHz to 40 kHz range. Of the two alternatives discrete solutions are usually less expensive because they do not include as many functions as the L296.

With the new L296 regulator the driving problem of the power control stage has been eliminated. Besides a higher overall efficiency, it is therefore also possible to operate directly at frequencies as high as 100 kHz. At 200 kHz the device still operates (further reducing the cost of the L and C external components) when a reduction of a few percent in efficiency is acceptable.

The device delivers a maximum current of 4A to the load, at an output voltage adjustable from 5.1 to 40V; the maximum operating input voltage is 46V. The high voltage and the high current capabilities of the device are a result of the special technology used and the special care taken in designing the power transistor. Essential requirements for a good power transistor are high gain and high current levels, low saturation voltage and good second breakdown robustness. To achieve high gain at high current levels, the power transistor has to be designed to maximize the emitter's perimeter/area ratio.

In the L296 power transistor, realized with a high voltage (50V) process, current densities in the magnitude order of 10 mA/Mil² are achieved.

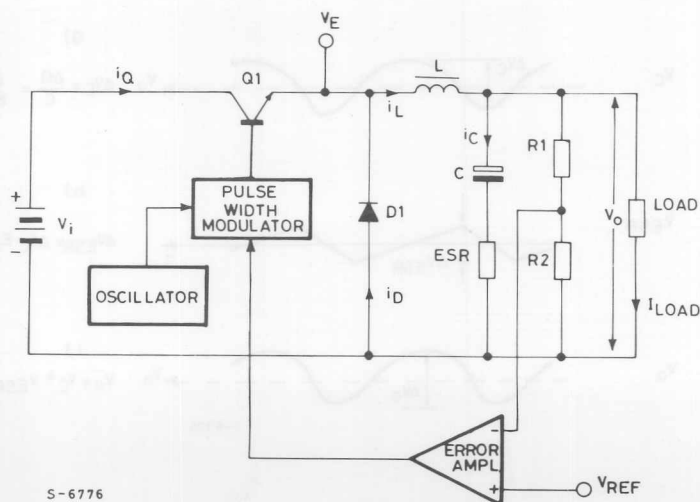
In its most complete configuration, in which all the available functions are being used, a significant reduction of the external component count is achieved compared with discrete component solution.

The L296 is mounted in a MULTIWATT® plastic package with 15 pins, minimizing the cost per watt and allowing a low thermal resistance of 3°C/W between junction and package and of 35°C/W between junction and ambient. This thermal resistance (including the contact resistance) is comparable to that of the more costly metal TO-3 packages.

THE STEP-DOWN CONFIGURATION

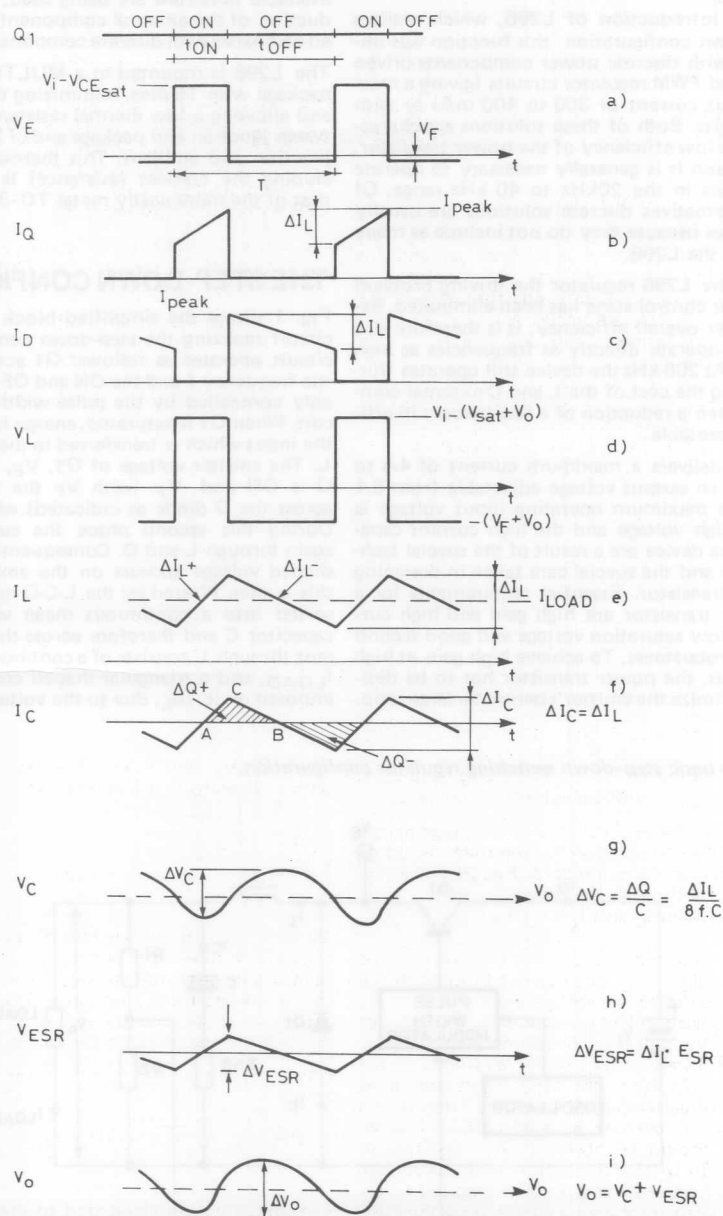
Fig. 1 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows: Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E , is $V_i - V_{sat}$ when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular-shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD} , and a triangular-shaped component superimposed on it, ΔI_L , due to the voltage across L.

Fig. 1 — The basic step-down switching regulator configuration.



S-6776

Fig. 2 — Principal circuit waveforms of the fig. 1 circuit.



S-6788

Fig. 2 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode are taken into account.

The ON and OFF times are established by the following expression:

$$V_o = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 2b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 2c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in fig. 2e. In balanced conditions the ΔI_L^+ current increase occurring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF} . The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula:

$$\begin{aligned} \Delta I_L^+ &= \Delta I_L^- = \frac{(V_i - V_{sat}) - V_o}{L} T_{ON} = \\ &= \frac{V_o + V_F}{L} T_{OFF} \end{aligned}$$

It is a good rule to respect to $I_{O_{MIN}} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 2d shows the behaviour of the voltage across coil L . In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 2f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD} .

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.

This ripple consists of two components: a capacitive component, ΔV_C , and a resistive component, ΔV_{ESR} , due to the ESR equivalent series resistance of the capacitor. Fig. 2g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that $v_C(t)$ is in quadrature with $i_C(t)$ and therefore with the voltage V_{ESR} . The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in fig. 2f:

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

which therefore gives:

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 2h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is $v_{ESR}(t) = i_C(t) \cdot ESR$. Fig. 2i shows the overall ripple V_o , which is the sum of the two previous components. As the frequency increases (> 20 kHz), which is required to reduce both the cost and the sizes of L and C , the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel to limit the value of ESR within the required level).

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in fig. 2 into account.

Starting from the initial conditions, where $Q = ON$, $v_C = V_o$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression:

$$V_i = v_L + v_C \quad (V_{sat} \text{ is neglected against } V_i).$$

$$V_i = L \frac{di_L}{dt} + v_C = L \frac{di_L}{dt} + V_o \quad (1)$$

which gives:

$$\frac{di_L}{dt} = \frac{(V_i - V_o)}{L} \quad (2)$$

The current through the inductance is given by:

$$I_L = \frac{(V_i - V_o)}{L} t \quad (3)$$

When V_i , V_o , and L are constant, I_L varies linearly with t . Therefore, it follows that:

$$\Delta I_L^+ = \frac{(V_i - V_o) T_{ON}}{L} \quad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot vary instantaneously, the voltage across the coil is inverted and the diode D becomes forward biased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present:

$$v_C(t) = V_o, \quad i_L(t) = i_D(t) = I_{peak}$$

And the equation associated to the following loop may be written:

$$V_F + L \frac{di_L}{dt} + v_C = 0 \quad (5)$$

where:

$$V_C = V_O$$

$$\frac{di_L}{dt} = -(V_F + V_O)/L \quad (6)$$

It follows therefore that:

$$i_L(t) = -\frac{V_F + V_O}{L} t \quad (7)$$

The negative sign may be interpreted with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_O , during the OFF time the following behaviour occurs:

$$i_L = \frac{V_O}{L} t \quad (8)$$

therefore:

$$\Delta i_L^- = \frac{V_O}{L} T_{OFF} \quad (9)$$

But, because

$$\Delta i_L^+ = \Delta i_L^- \quad \text{it follows that :}$$

$$\frac{(V_i - V_O) T_{ON}}{L} = \frac{V_O T_{OFF}}{L}$$

which allows us to calculate V_O :

$$V_O = V_i \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i \frac{T_{ON}}{T} \quad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_O to the input voltage V_i and to the duty cycle. The relationship between the currents is the following:

$$i_{DC} = i_{oDC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula:

$$\eta \% = \frac{P_o}{P_i} 100$$

$$\text{where } P_o = V_o i_o \quad (\text{with } i_o = i_{LOAD})$$

is the output power to the load and P_i is the input

power absorbed by the system. P_i is given by P_o , plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + P_{sw}} \quad (12)$$

DC LOSSES

P_{sat} : saturation losses of the power transistor Q_1 . These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot i_o \frac{T_{ON}}{T} = V_{sat} i_o \frac{V_o}{V_i} \quad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power transistor saturation at current i_o .

P_D : losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F i_o \frac{V_i - V_o}{V_i} = V_F i_o (1 - \frac{V_o}{V_i}) \quad (14)$$

where V_F is the forward voltage of the recirculation diode at current i_o .

P_L : losses due to the series resistance R_S of the coil

$$P_L = R_S i_o^2 \quad (15)$$

P_q : losses due to the stand-by current and to the power driving current:

$$P_q = V_i i'_{3q} + V_i i''_{3q} \frac{T_{ON}}{T} \quad (16)$$

where being:

$$\frac{T_{ON}}{T} = \frac{V_o}{V_i} \quad \text{it follows that :}$$

$$P_q = V_i i'_{3q} + V_o i''_{3q} \quad \text{in which :}$$

$$i'_{3q} = i_{3q} \quad \text{at 0\% duty cycle}$$

$$i''_{3q} = i_{3q(100\% d.c.)} - i_{3q(0\% d.c.)}$$

SWITCHING LOSSES

P_{sw} : switching losses of the power transistor:

$$P_{sw} = V_i i_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are

neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_O) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculating T_{ON} and T_{OFF} through (4) and (9) respectively it follows that:

$$T_{ON} = \frac{\Delta I_L^+ \cdot L}{V_i - V_o} \quad T_{OFF} = \frac{\Delta I_L^- \cdot L}{V_o}$$

But because:

$$T_{ON} + T_{OFF} = T \quad \text{and} \quad \Delta I_L^+ = \Delta I_L^- = \Delta I_L$$

it follows that:

$$\frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T$$

Calculating L, the previous relation becomes:

$$L = \frac{(V_i - V_o) V_o}{V_i \Delta I_L} T \quad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_O), and introducing the frequency instead of the period, it follows that:

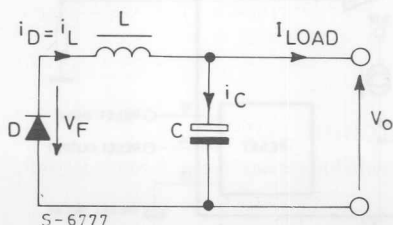
$$L = \frac{(V_i - V_o) V_o}{V_i \cdot 0.3 \cdot I_O \cdot f} \quad \text{where } L \text{ is in Henry and } f \text{ in Hz}$$

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by:

$$i_C(t) = i_L(t) - I_O$$

Fig. 3 — Equivalent circuit showing recirculation when Q_1 is turned off.



From the behaviour shown in fig. 2 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time $T/2$. It follows therefore that:

$$\Delta V_C = \frac{\Delta I_L}{4C} \cdot \frac{T}{2} = \frac{\Delta I_L T}{8C} = \frac{\Delta I_L}{8fC} \quad (19)$$

but, remembering expression (4):

$$\Delta I_L^+ = \frac{(V_i - V_o) T_{ON}}{L} \quad \text{and} \quad T_{ON} = \frac{V_o}{V_i} T$$

therefore equation (19) becomes:

$$\Delta V_C = \frac{(V_i - V_o) V_o}{8 V_i f^2 L C}$$

Finally, calculating C it follows that:

$$C = \frac{(V_i - V_o) V_o}{8 V_i \Delta V_C f^2 L} \quad (20)$$

where:
 L is in Henrys
 C is in Farads
 f is in Hz

Finally, the following expression should be true:

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \quad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_C = C(dv_C/dt)$ (22), where $dv_C = \Delta V_O$, the instantaneous variation of the load current ΔI_O is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.

Moreover, the following is true:

$$v_L = L \frac{di_L}{dt} \quad (23) \quad \text{where } di_L = \Delta I_O$$

$$v_L = V_i - V_o \quad \text{for a load increase}$$

$$v_L = V_o \quad \text{for a load decrease}$$

Calculating dt from (22) and (23) and equalizing, it follows that:

$$L \frac{di_L}{v_L} = C \frac{dv_C}{i_C}$$

Calculating dv_C and equalizing it to ΔV_O , it follows that:

$$\Delta V_O = \frac{L \Delta I_O^2}{C(V_i - V_O)} \quad (24) \quad \text{for } +\Delta I_O$$

$$\Delta V_O = \frac{L \Delta I_O^2}{C V_O} \quad (25) \quad \text{for } -\Delta I_O$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_O it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the undershoot, which could trigger the reset function.

DEVICE DESCRIPTION

Fig. 4 shows the package in which the device is mounted and the pin function assignments. The internal structure of the device is shown in fig. 5. Each block will now be examined.

Power supply

The device is provided with an internal stabilized power supply that, besides supplying the reference voltage of 5.1V for the whole system, also supplied the internal analog blocks.

Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zener-zap trimming, the voltage is within $\pm 2\%$ limits.

Fig. 4 – Pin assignments of the L296.

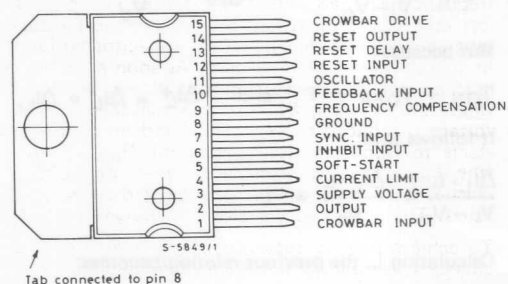
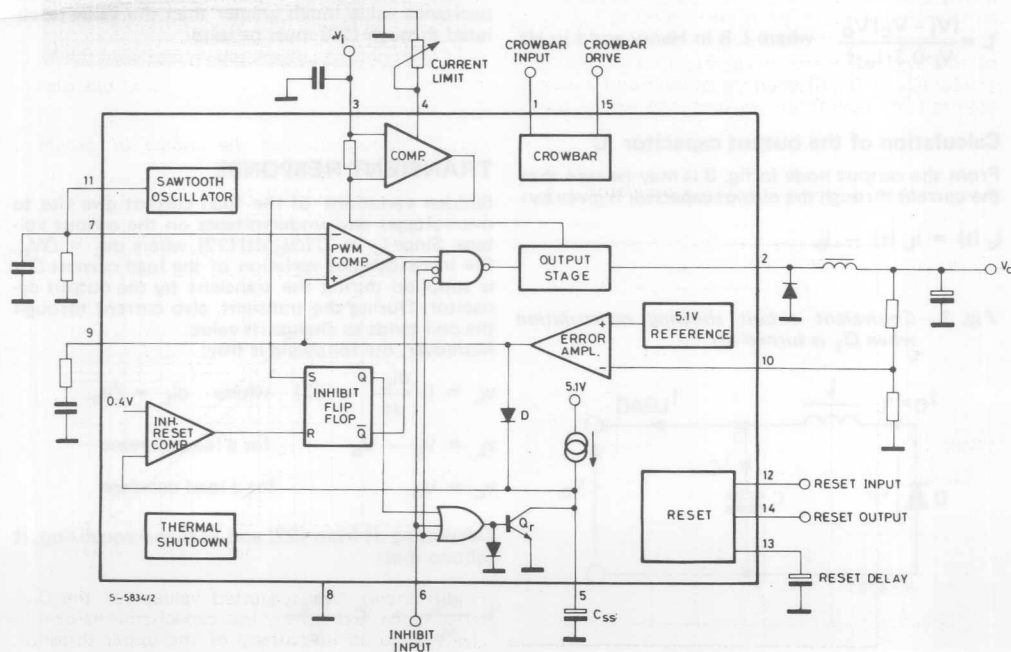


Fig. 5 – Block diagram of the L296. In addition to the basic regulation loop the device includes functions such as reset, crowbar and current limiting.



OSCILLATOR

The oscillator block generates the saw-tooth waveform that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The saw-tooth, whose amplitude is between 1.2V and 3.2V, is generated by charging rapidly the C_{OSC} capacitor which then discharges across the R_{OSC} resistance. As shown in fig. 6, the oscillator is realized by a comparator (with grounded compatible input) with hysteresis whose thresholds are 1.2V and 3.2V respectively. The C_{OSC} capacitor and the R_{OSC} resistance are connected to the non-inverting input of the comparator which set the oscillating frequency is fixed. When the voltage on pin 11 is less than 3.2V, the switch S_1 is closed and the current generator charges the C_{OSC} capacitor rapidly; in this phase S_2 is also closed. As soon as 3.2V is reached the comparator output drives S_2 open (therefore opening S_1 , too); the inverting input voltage is reduced to about 1.2V and the capacitor starts to discharge itself across the R_{OSC} resistor (the I_{bias} effect is neglected). When the voltage reaches 1.2V, S_2 and S_1 close again and a new cycle starts. The generated waveform is shown in fig. 7.

To achieve a good accuracy of the switching frequency it is essential to have a charging time of the capacitor which is much smaller than the discharging time. In this way, the oscillation frequency only depends on the external components C_{OSC} and R_{OSC} . For this reason the capacitor charging current (when S_1 is ON) is typically around 10 mA. For example, with a 2.2 nF capacitor to switch from 1.2V to 3.2V about 400 ns is required, which is negligible compared to the 10 μ s period that occurs when the operation is performed at 100 kHz. The diagrams shown in fig. 8 allow the calculation of the R_{OSC} value (R_1 in fig. 8) with C_{OSC} as a parameter (C_3 in fig. 8) when the oscillation frequency required for operation has been previously fixed.

Fig. 6 – Internal schematic of the oscillator

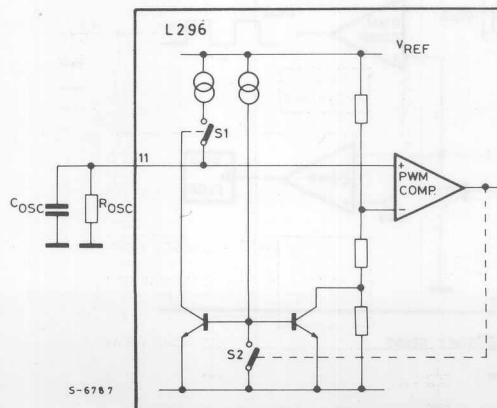


Fig. 7a – Oscillator waveform at pin 11 with $f = 100$ KHz ($R_{OSC} = 4.3$ K Ω , $C_{OSC} = 2.2$ nF)

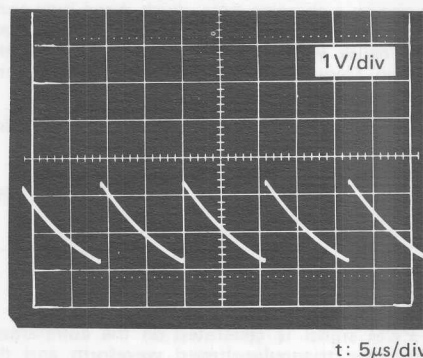


Fig. 7b – Oscillator waveform at pin 11 with $f = 50$ KHz ($R_{OSC} = 9.1$ K Ω , $C_{OSC} = 2.2$ nF)

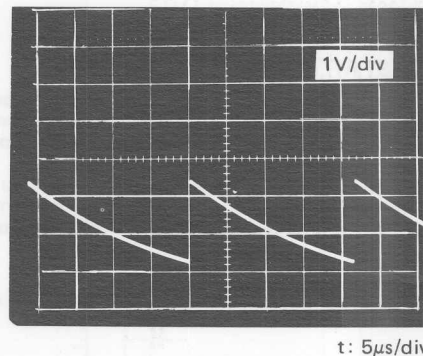


Fig. 8 – Nomogram for the choice of oscillator components.

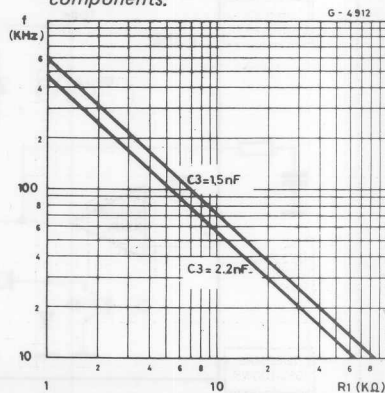


Fig. 8 shows two suggested values for the C_{OSC} capacitance. Excessively low capacitance value may give rise to an inaccuracy of the upper threshold

due to the switching delays of the comparator. This inaccuracy is caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too long compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to spread of the charge current.

The oscillation frequency is given by the following formula:

$$f_{osc} = \frac{1}{R_{osc} C_{osc}} \quad (26)$$

PWM (see fig. 9)

The PWM signal is generated on the comparator output; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

SOFT START (see fig. 9)

Soft start is an essential function for correct start-up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage. In particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a

steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limitation and after the intervention of the thermal protection.

The soft-start function is realized through a capacitor connected to pin 5 which is charged at constant current ($\cong 100\mu A$) up to a value of about V_{REF} . During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp; the power stage starts to switch with steadily increasing duty cycle. This behaviour is shown in fig. 10. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF} .

The soft-start effect is determined, apart from the switch-on time, when the current limitation operates, due to either an overload or a short circuit, to keep the mean value of the current absorbed by the power supply low.

Moreover from fig. 11 it may be observed that since the voltage on pin 9 can decrease under the minimum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Fig. 9 — Partial internal schematic showing PWM and soft start blocks.

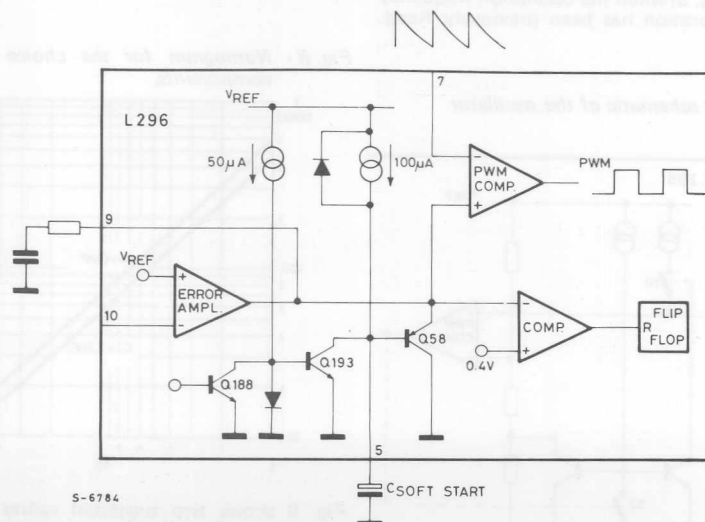


Fig. 10 — Soft start waveforms. When power is applied, or after an inhibit, the L296's output current rises slowly under control of the soft start circuit.

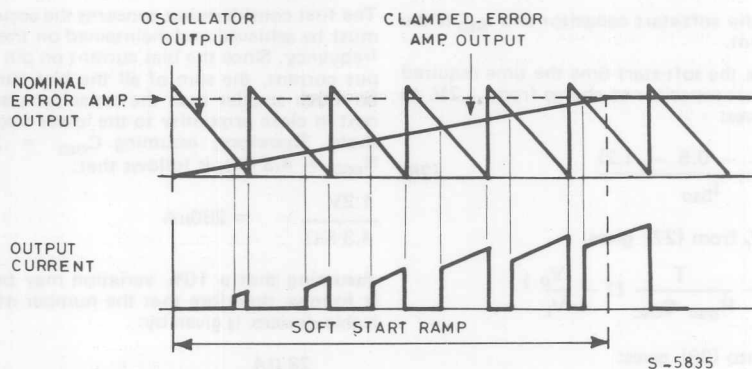
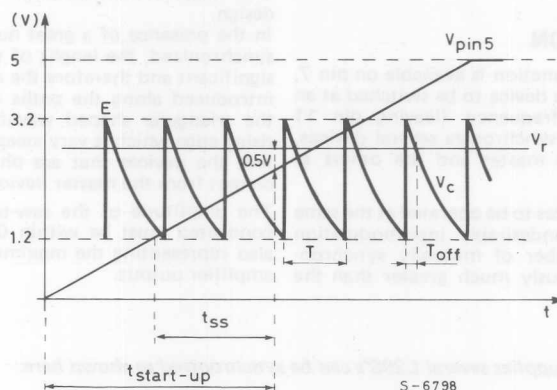


Fig. 11 — Waveform for calculation of duty cycle and soft start time.



CALCULATING THE DUTY CYCLE AND SOFT-START TIME

Assume, for simplicity, that the rising edge of the ramp is instantaneous; V_r is the output voltage of the error amplifier and V_c the ramp voltage (see fig. 11). The PWM comparator block switches when $V_r = V_c$; therefore:

$$V_r = V_c = E e^{-\frac{t}{R_{osc} C_{osc}}}$$

Consequently:

$$t = R_{osc} C_{osc} \ln \frac{E}{V_r}$$

The time obtained from this expression is the T_{OFF} time of the power transistor. The duty cycle d is given by:

$$d = \frac{T_{ON}}{T} = \frac{T - R_{osc} C_{osc} \ln \frac{E}{V_r}}{T} = 1 - \frac{R_{osc} C_{osc} \ln \frac{E}{V_r}}{T} = \frac{V_o}{V_i} \quad (27)$$

Consequently, starting with the capacitor discharged, the output of the regulator will be at the nominal level when the voltage at the terminal of the capacitor (which is charged by a constant current) has reached $V_r - 0.5V$.

$$t_{\text{start-up}} = \frac{C_{ss} (V_r - 0.5V)}{I_{5so}}$$

where C_{ss} is the soft-start capacitor and I_{5so} is the charging current.

Considering as the soft-start time the time required for the soft-start capacitor to charge from 1.2V to $V_r - 0.5V$, gives:

$$t_{ss} = \frac{C_{ss} (V_r - 0.5 - 1.2)}{I_{5so}} \quad (28)$$

substituting V_r from (27) gives:

$$V_r = E e^{-\frac{T}{R_{osc} C_{osc}}} \left(1 - \frac{V_o}{V_i}\right)$$

substituting into (28) gives:

$$t_{ss} = \frac{C_{ss}}{I_{5so}} \left(E e^{-\frac{T}{R_{osc} C_{osc}}} \left(1 - \frac{V_o}{V_i}\right) - 1.7 \right)$$

SYNCHRONIZATION

The synchronization function is available on pin 7, this function allows the device to be switched at an externally generated frequency (leaving pin 11 open), or to mutually synchronize several devices, using one of them as master and the others as slave (Fig. 12).

This allows several devices to be operated at the same frequency, avoiding undesirable intermodulation phenomena. The number of mutually synchronizable devices is obviously much greater than the

three devices shown in the figure. It is anyway difficult to establish an exact maximum number of devices, as it depends on different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming $C_{osc} = 2.2 \text{ nF}$ and $R_{osc} = 4.3 \text{ K}\Omega$, it follows that:

$$\frac{1.2V}{4.3 \text{ K}\Omega} = 280 \mu A$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by:

$$N = \frac{28 \mu A}{I_{bias \text{ max}}}$$

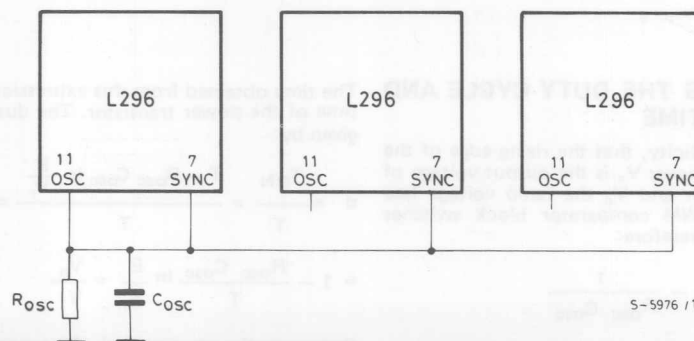
This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.

In the presence of a great number of devices to be synchronized, the length of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be within 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

Fig. 12 — In multiple supplies several L296's can be synchronized as shown here.



CURRENT LIMITATION

The current limitation function has been realized in a rather innovative way to avoid overload condition during the short circuit operation. In fact, while for all the other devices a constant current limitation is implemented by acting on the duty cycle (therefore, in short circuit conditions an output current is equal to the maximum limitation current), the new control approach allows operation in short circuit conditions with a mean current much smaller than the allowed 4A value. Operation of the current limiter will now be described.

Refer to the block diagram, fig. 13.

The current which is delivered from the output transistor to the load flows through the current sensing resistor R_S . When the voltage drop on R_S is equal to the offset voltage of the current comparator, the comparator generates a set pulse for the flip-flop, with a delay of about 1 μ sec. The purpose of this delay is to avoid triggering of the protection circuit on the current peak that occurs during the recirculation phase. Therefore, the output Q goes

low and the power stage is immediately switched off, while the output Q goes high and acts directly on the soft-start capacitor discharging the soft-start capacitor at a constant current (about 50 μ A).

When the voltage on pin 5 reaches 0.4V the comparator triggers, supplying a reset pulse to the flip-flop; from now on, the power stage is enable and the soft-start phase starts again. When the limitation cause, either overload or short circuit, is still present the cycle repeats again. The waveform of the output current on pin 2 is shown in fig. 14.

From fig. 14 it may be observed how this current limitation technique allows the short circuit operation with a very low output current value.

It is possible to reduce the maximum current value by acting on pin 4. On this pin a voltage of about 3.3V is present; by connecting a resistance a constant current, given by $3.3/R$, is sent to ground. This current reduces the offset voltage of the current comparator, therefore anticipating its triggering threshold.

Fig. 13 — Partial schematic showing the current limiter circuit.

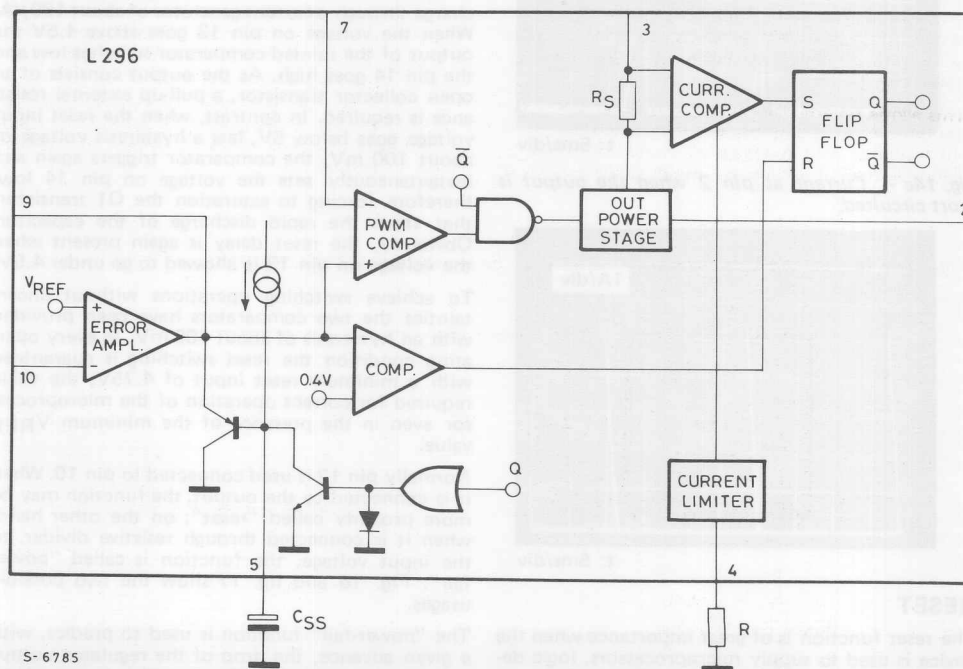


Fig. 14a — Current limiter waveforms.

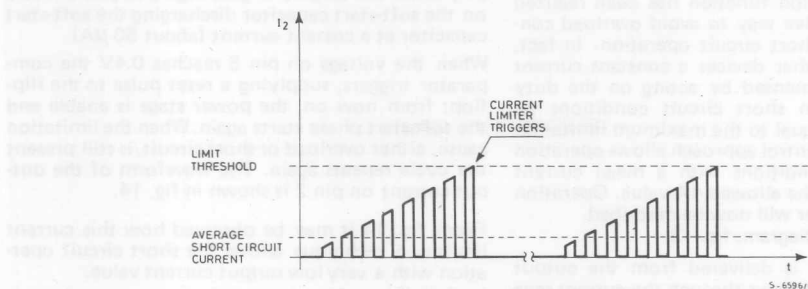


Fig. 14b — Load current in short circuit conditions ($V_i = 40V$, $L = 300 \mu H$, $f = 100 KHz$)

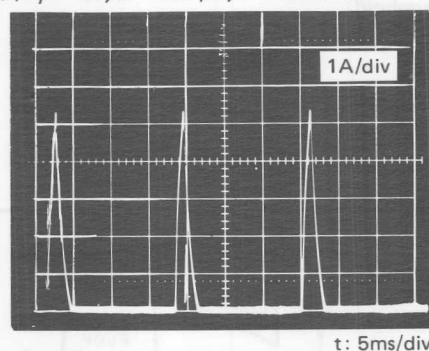
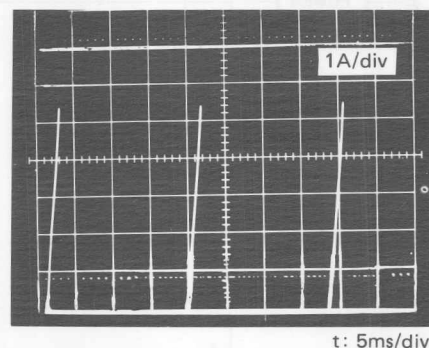


Fig. 14c — Current at pin 2 when the output is short circuited.



RESET

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the SGS L296 device from all previous devices. The block diagram of the function is shown in fig. 15. A reset signal is generated when the output voltage

is within the limits required to supply the microprocessor correctly.

The reset function is realized through the use of 3 pins: the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is saturated and the voltage on pin 14 is at low level, since Q2 is saturated, too. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about $100 \mu A$. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up external resistance is required. In contrast, when the reset input voltage goes below 5V, less a hysteresis voltage of about 100 mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100 mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called "reset"; on the other hand, when it is connected through resistive divider, to the input voltage, the function is called "power fail". Fig. 16 and fig. 17 show the two possible usages.

The "power-fail" function is used to predict, with a given advance, the drop of the regulator output voltage, due to main failures, which is enough to save the data being processed into protected memory areas. Fig. 18 summarises the reset function operation.

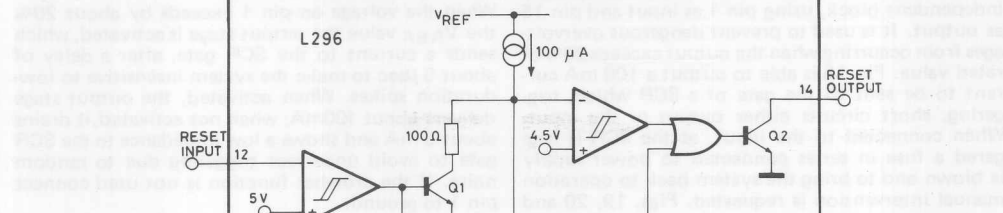
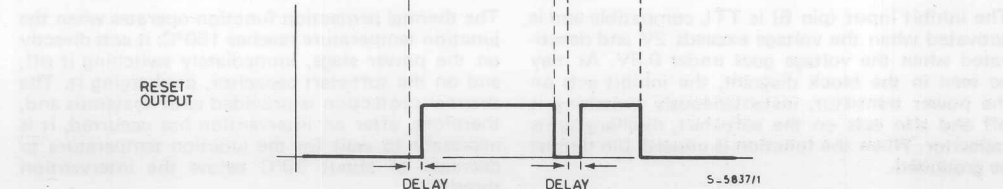
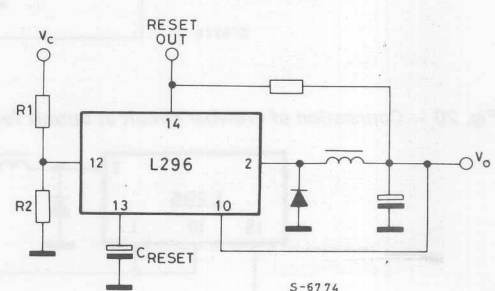


Fig. 17 — To obtain a power fail signal, the reset block is connected like this.



CROWBAR

This protection function is realized by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous overvoltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100 mA current to be sent to the gate of a SCR which, triggering, short circuits either output or the input. When connected to the output, as the SCR is triggered a fuse in series connected to power supply is blown and to bring the system back to operation manual intervention is requested. Figs. 19, 20 and

21 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about 5 μ sec to make the system insensitive to low-duration spikes. When activated, the output stage delivers about 100mA; when not activated, it drains about 5 mA and shows a low impedance to the SCR gate to avoid uncorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

Fig. 19 — Connection of crowbar circuit at output for 5.1V output applications.

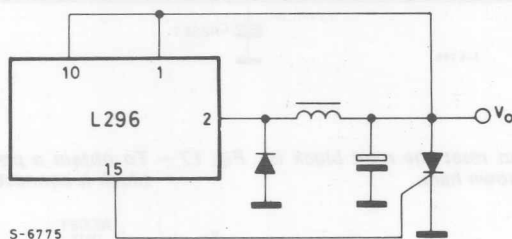


Fig. 20 — Connection of crowbar circuit at output for output voltages above 5.1V.

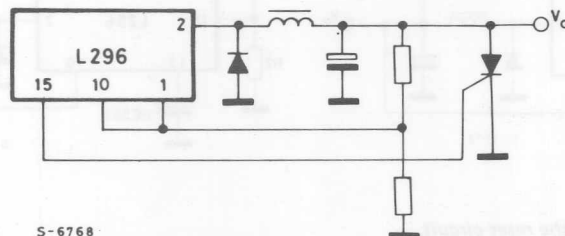
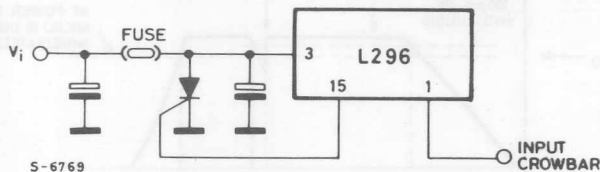


Fig. 21 — Connection of crowbar circuit to protect input. When triggered, the SCR blows the fuse.



INHIBIT

The inhibit input (pin 6) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C; it acts directly on the power stage, immediately switching it off, and on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

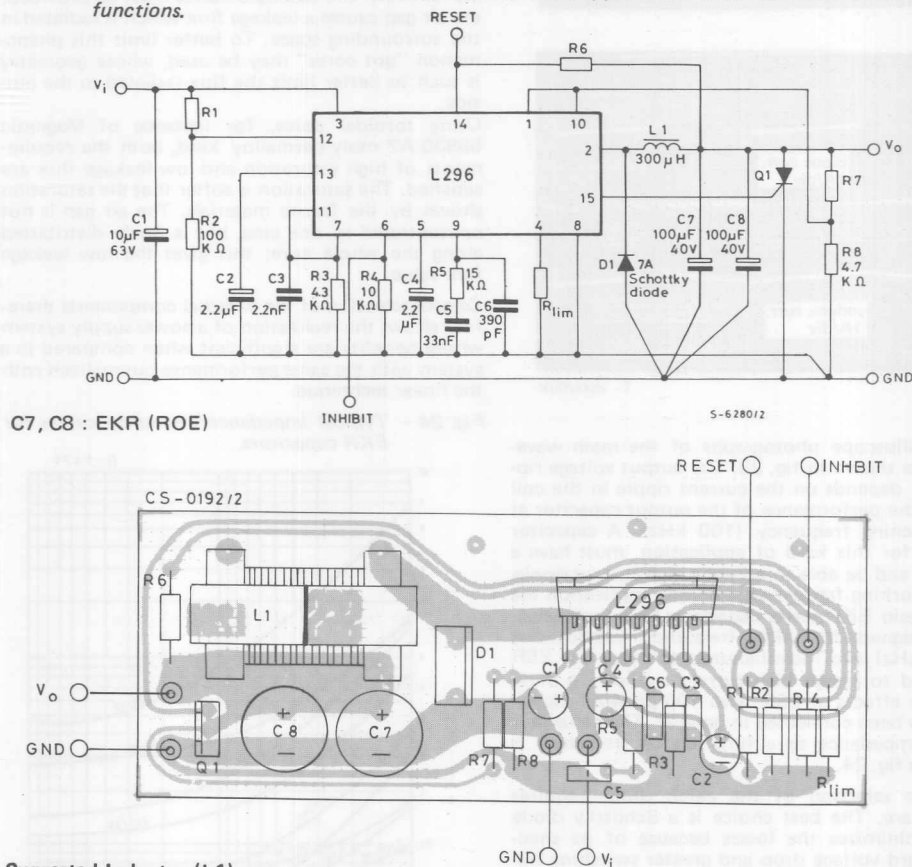
Though the L296 is designed for step-down regulator configurations it may be used in a variety of other applications. We will now examine these possibilities and show how the capabilities of the device may be extended.

In fig. 22 the complete typical application is shown, where all the functions available on the device are being used. This circuit delivers to the load a maximum current of 4A and a voltage which is established by the voltage divider constituted by R_7 and R_8 resistances. The following table is helpful for a quick calculation of some standard output voltages:

Resistor value for standard output voltages		
V_o	R_8	R_7
12V	4.7 k Ω	6.2 k Ω
15V	4.7 k Ω	9.1 k Ω
18V	4.7 k Ω	12 k Ω
24V	4.7 k Ω	18 k Ω

To obtain $V_o = V_{REF}$ the pin 10 is directly connected to the output, therefore eliminating both R_7 and R_8 . The switching frequency is 100 kHz.

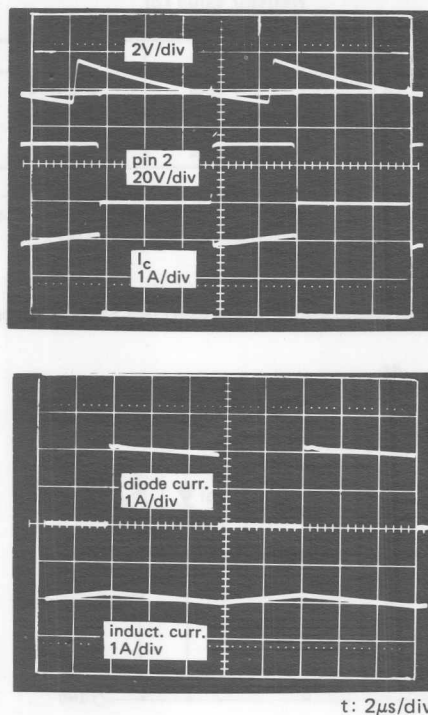
Fig. 22 — Schematic, PCB layout and suggested component values for the evaluation circuit used to characterize the L296. This is a typical stepdown application which exercises all the device's functions.



Suggested Inductor (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	—
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633& - G0500 - X127)	40	2 x 0.8 mm.	—
VOGT 250 µH Toroidal coil, part number 5730501800			

Fig. 23 — Oscilloscope photographs showing main waveforms of the figure 22 circuit.



The oscilloscope photographs of the main waveforms are shown in fig. 23. The output voltage ripple ΔV_O depends on the coil and on the performance of the output capacitor at the switching frequency (100 kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. For this application the Roederstein EKR series capacitors have been selected, designed for high frequency applications (>200 kHz) and manufactured to show low ESR value and to accept high current ripples. To minimize the effects of ESR, two 100 μ F/40V capacitors have been connected in parallel. The behaviour of the impedance as a function of frequency is shown in fig. 24.

Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimizes the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.

When the full input voltage range of the device is required in this application it is possible to use super fast diodes with 35 to 50 ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes,

with $t_{rr} = 100$ ns or more is not recommended; The photographs in fig. 25 show the effects on the power current and on the voltage on pin 2, due to the diodes showing different speeds. Diodes showing t_{rr} greater than 35-50 ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

The third component requiring care is the inductor. Fig. 22a shows the part numbers of some types used for testing. Besides having the required inductance value, the coil has to show a very high saturation current.

Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L} , the current limit threshold.

To achieve high saturation with ferrite cores an air gap between the two core halves must be provided; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon "pot cores" may be used, whose geometry is such to better limit the flux radiated to the outside.

Using toroidal cores, for instance of Magnetic 58930-A2 moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer than the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core; this gives the low leakage flux value.

Careful selection of the external components therefore allows the realization of a power supply system whose benefits are significant when compared to a system with the same performance but realized with the linear technique.

Fig. 24 — Typical impedance/frequency curves for EKR capacitors.

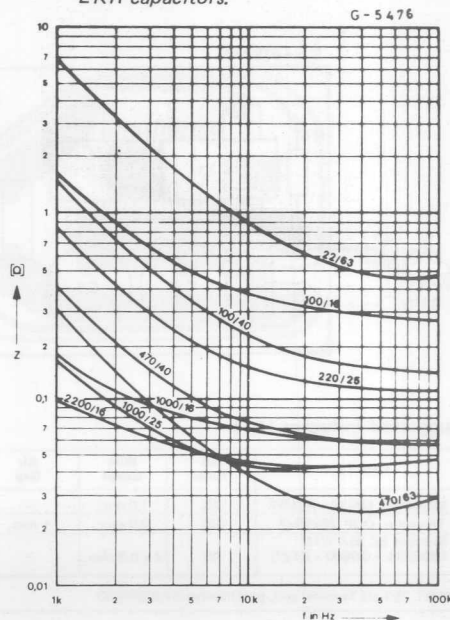
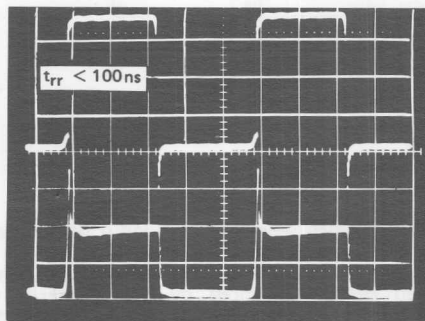
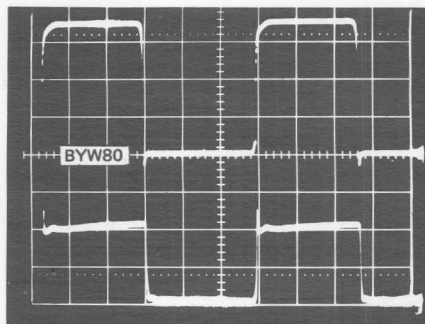
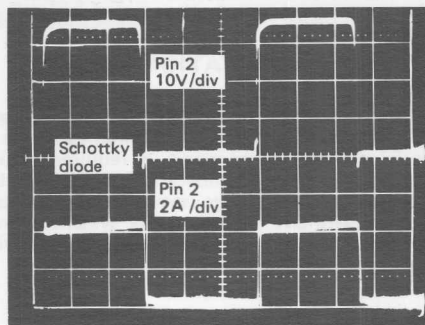


Fig. 25 — Oscilloscope photographs showing the waveforms obtained with diodes having different t_{rr} values.



t: 2μs/div

SWITCHING vs LINEAR

Switching regulators are more efficient than linear types so the transformer and heatsink can be smaller and cheaper. But how much can you gain?

We can estimate the savings by comparing equivalent linear and switching regulators. For example, suppose that we want a 4A/5V supply.

Linear

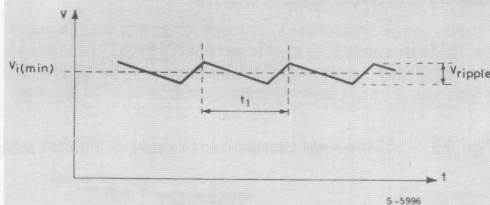
For a good linear regulator the minimum dropout

will be at least 5V at 4A. The minimum input voltage is given by:

$$V_{i \min} = V_o + V_{\text{drop}} + \frac{1}{2} V_{\text{ripple}}$$

where:

$$V_{\text{ripple}} \approx \frac{I_o t_1}{C} = \frac{4 \times 8 \times 10^{-3}}{10 \times 10^{-3}} = 3.2V$$



(a good approximation is 8 ms for t_1 at mains frequency of 50Hz) and 10,000 μF for C, the filter capacitor after the bridge). Therefore $V_{i \min} \approx 10.6V$. Since operation must be guaranteed even when the mains voltage falls 20%, the nominal voltage on load at the terminals of the regulator must be:

$$V_{\text{nom}} = \frac{V_{i \min}}{0.8} = \frac{10.6}{0.8} = 13.25V$$

To allow even a small margin we have to choose:

$$V_{\text{nom}} = 14V$$

The power that the series element must dissipate is therefore:

$$P_d = (V_{\text{nom}} - V_o) I_o = 36W$$

and a heatsink will be necessary with a thermal resistance of:

$$R_{\text{th heats.}} = 0.8^\circ\text{C/W}$$

and the transformer must supply a power of:

$$P_{\text{diss}} = 14 \times 4 = 56W$$

It must therefore be dimensioned for:

$$P_D = \frac{56}{0.9} = 62VA$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements; the L296 itself and the recirculation diode.

It follows that the transformer must be roughly 30VA and the heatsink thermal resistance about 11 °C/W.

	Linear	Switching
Transformer	62 VA	30 VA
Heatsink	0.8 °C/W	11 °C/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80–90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower – particularly when the circuit is enclosed in a box – with all the

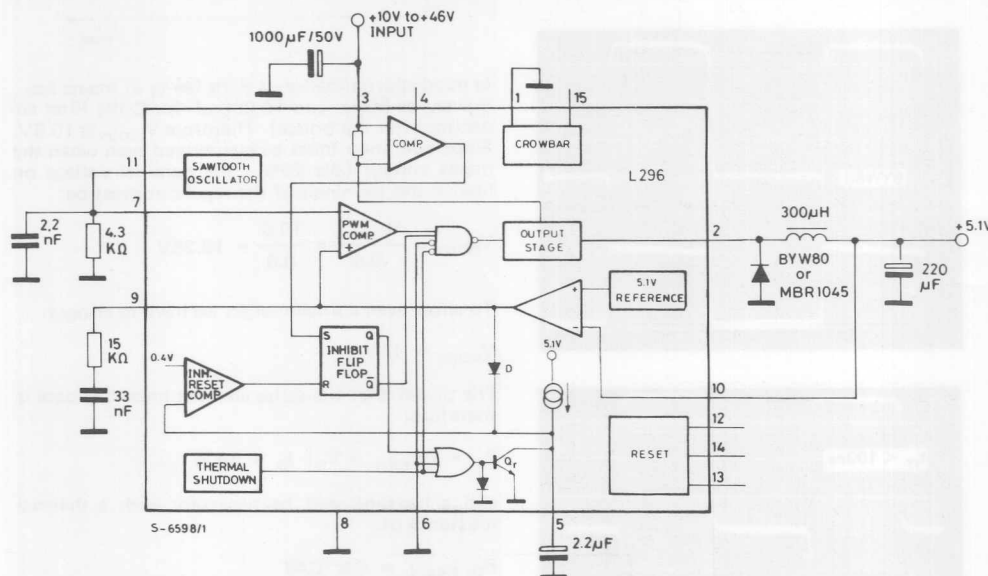
advantages cooler operation brings.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

LOW COST APPLICATION AND PREREGULATOR

Fig. 26 shows the low cost application of a 4A and $V_O = 5.1V$ power supply. A minimum amount of essential external components is required, which are necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

Fig. 26 – A minimal component count 5.1V/4A supply.



This application is very well suited not only as a low-cost power supply, but also as pre-regulator for post-regulators distributed in different circuit points, or even on different boards (Fig. 27). The post-regulators may be selected among the low-drop types, like L4805 and L387 for example, still obtaining a high efficiency, combined with an excellent regulation. The use of L387 device allows us to use also the reset function, useful to power a microprocessor.

POWER SUPPLY COMPLETE WITH TRANSFORMER

Fig. 28 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

As already stated above, the output capacitors have to show some special features, like low ESR and high current ripple, to obtain low voltage ripple

values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300 µF/50V EYF (ROE) capacitors have been used.

POWER SUPPLY WITH MAINS SWITCHING PREREGULATOR

When it is desirable to eliminate the 50/60 Hz transformer – in portable or volume-limited equipment – a mains preregulator can be added to reduce the input voltage to a level acceptable for the L296.

In this case the pre-regulator circuit is connected to the primary of the transformer which now operates at the switching frequency and is therefore smaller and lighter.

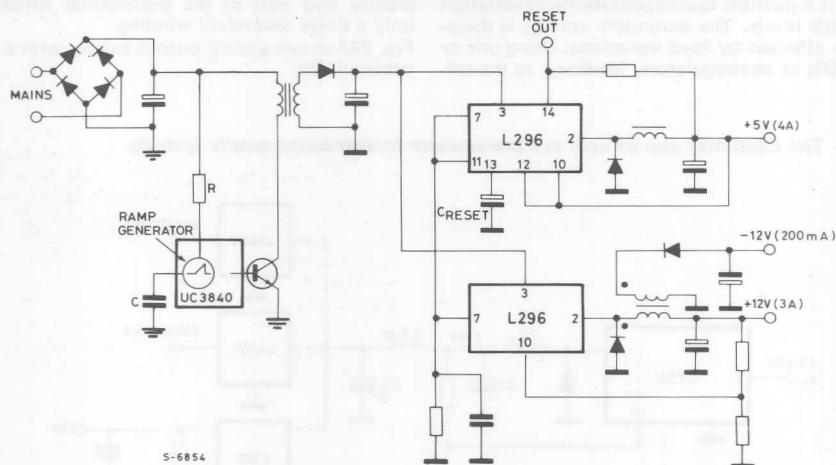
Fig. 28A shows a multi-output supply with a mains preregulator.

The diagram shows a power supply circuit. An input of 10-40V V_I is connected to pin 3 of the L296. Pin 10 of the L296 is connected to ground. Pin 2 of the L296 is connected to a diode (cathode to ground) and inductor L1. The other end of L1 is connected to a 5.8V reference voltage, which is also connected to pin 5 of the L296. A capacitor C1 is connected between the 5.8V line and ground. Inductor L2 is connected between the 5.8V line and the input of the first L4805 regulator. A capacitor C2 is connected between the input of the first L4805 and ground. The first L4805 is configured as a 5V/400mA regulator. Its output is connected to the input of the second L4805, which is also configured as a 5V/400mA regulator. The output of the second L4805 is connected to the input of the L387 regulator. The L387 is configured as a 5V regulator. Its output is connected to a 5V output terminal and a RESET OUTPUT signal terminal. A dashed box indicates a connection between the RESET OUTPUT and the L387. A note at the bottom states: * L2 and C2 are necessary to reduce the switching frequency spikes.

[illegible]

21

Fig. 28A — A multiple output supply using a switching preregulator rather than a mains transformer.



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POWER SUPPLY WITH 0 – 30V ADJUSTABLE VOLTAGE

When output voltages lower than 5V are required, the circuit shown in fig. 29 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10 kΩ resistor is fixed at approximately 2.5 mA to obtain an output voltage of 30V. The equivalent circuit is shown in fig. 30.

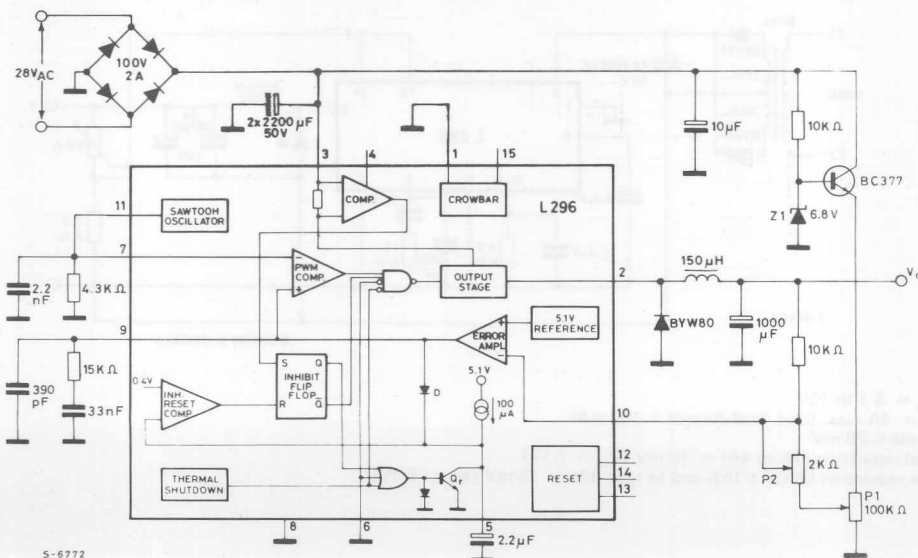
Acting now on the slider of P1, the current flow-

ing through the divider may be varied. The new equivalent circuit is shown in fig. 31.

Reducing the current flowing, also the voltage drop across the 10 kΩ resistance is reduced, together with V_O . When the current reaches zero, it follows that $V_O = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF} , the current start to flow in opposite direction and V_O begins to decrease below 5V.

When $I_1 \times 10K\Omega = V_{REF}$ it follows that $V_O = 0$.

Fig. 29 — Variable 0–30 V supply illustrating how output voltages below 5.1V are obtained.



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Fig. 30 — When setting up the figure 29 circuit the slider of P1 is grounded, giving the equivalent circuit shown here, and P2 adjusted to give an output voltage of 30 V.

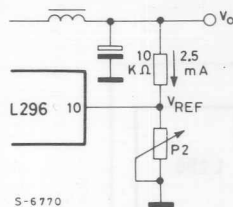


Fig. 31 — Partial schematic showing output voltage adjustment of figure 29.

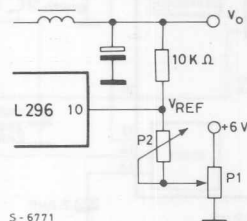
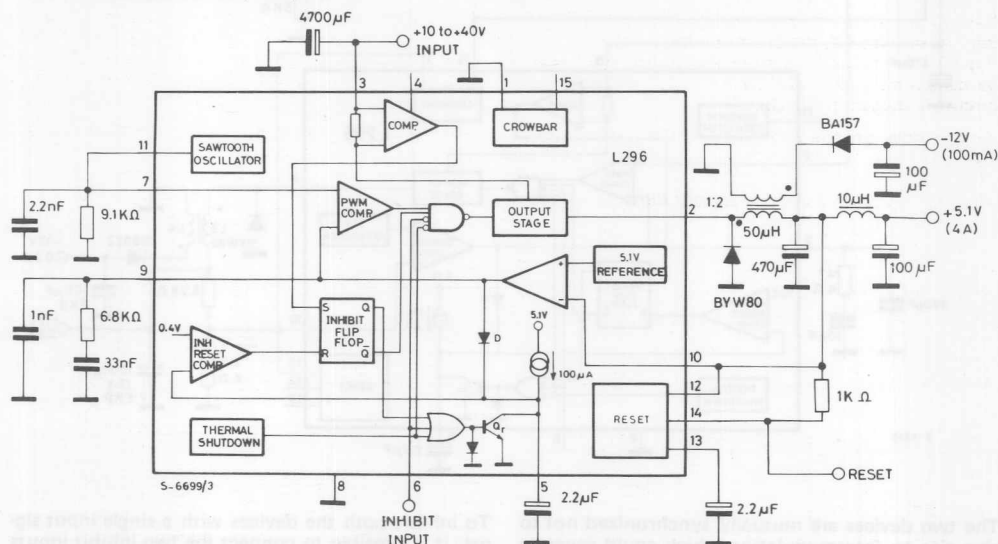


Fig. 32 — Dual output regulator showing how an additional winding can be added to the inductor to generate a secondary output.



PERSONAL COMPUTER POWER SUPPLY

Using two mutually synchronized devices it is possible to obtain a four output power supply suitable for power a microprocessor system.

- $V_{01} = 5.1V/4A$
- $V_{02} = 12V/2.5A$ (up to 4A)
- $V_{03} = -5V/0.2A$
- $V_{04} = -12V/0.2A$

DUAL OUTPUT REGULATOR

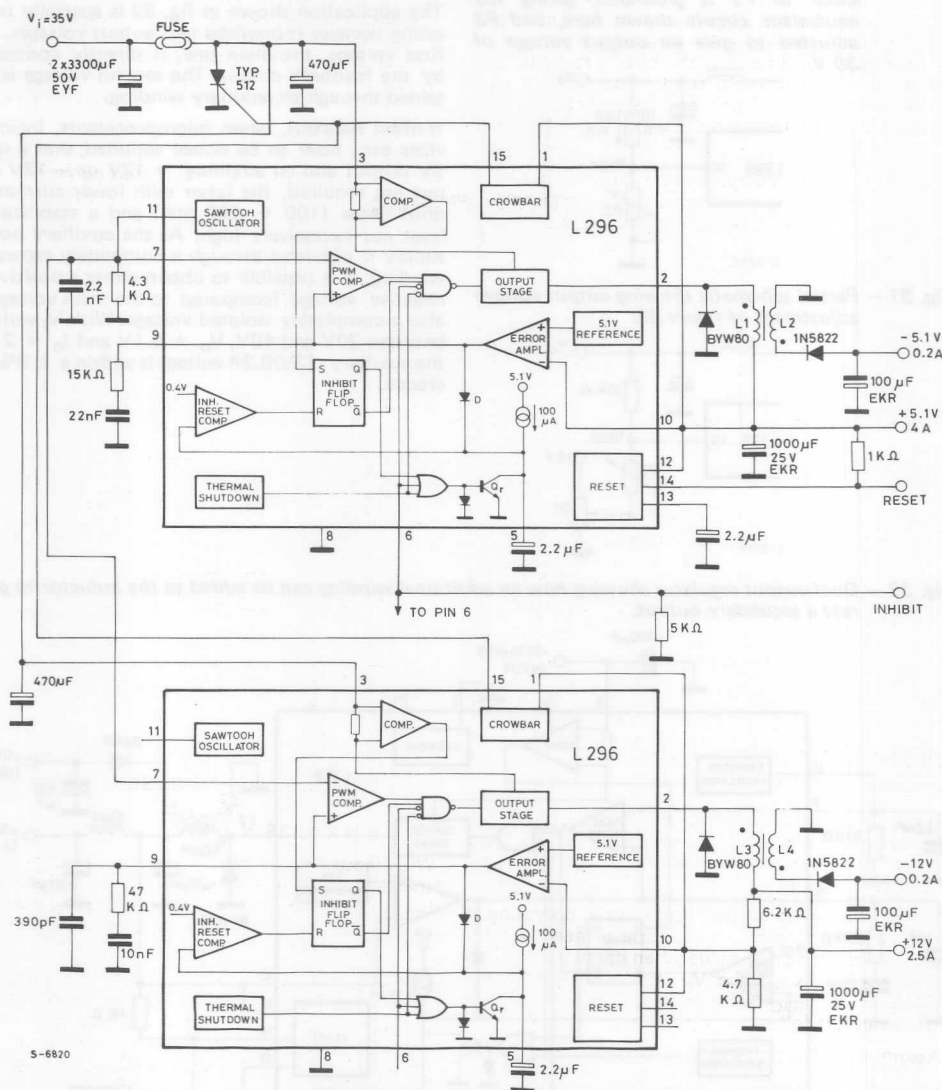
The application shown in fig. 32 is specially interesting because it provides two output voltages. The first voltage, the main one, is directly controlled by the feedback circuit. The second voltage is obtained through an auxiliary winding.

It often happens, when microprocessors, logic devices etc., have to be power supplied, that a main 5V output and an auxiliary +12V or -12V output are required, the latter with lower current requirements (100 ÷ 200 mA) and a stabilization level not excessively high. As the auxiliary power supply is obtained through a completely separated winding, it is possible to obtain either a positive or negative voltage (compared to the main voltage) or also a completely isolated voltage. With V_i variable between 20V and 40V, $V_o = 5.1V$ and $I_o = 2.5A$, the auxiliary -12V/0.2A voltage is within a $\pm 2\%$ tolerance.

The schematic diagram is shown in fig. 33. The 5V output is also provided with the reset function, that is available also for the 12V output.

The feedback is direct, no other external component is used and no calibration is therefore required. An output is obtained with the accuracy of the reference voltage ($\pm 2\%$). For the 12V output, by using a resistive divider with 1% resistance an output is obtained whose spread is within $\pm 4\%$.

Fig. 33 — Microcomputer supply with 5V, -5V, 12V and -12V outputs.



The two devices are mutually synchronized not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the devices power supply. In this way, should a faulty be present on either of the main outputs, the supply is switched off for whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together; the 5K Ω resistance is used when the inhibit input is left open. If this input is not used it must be grounded.

As may be noted in the diagram, to obtain the two auxiliary voltages is very simple and cost-effective.

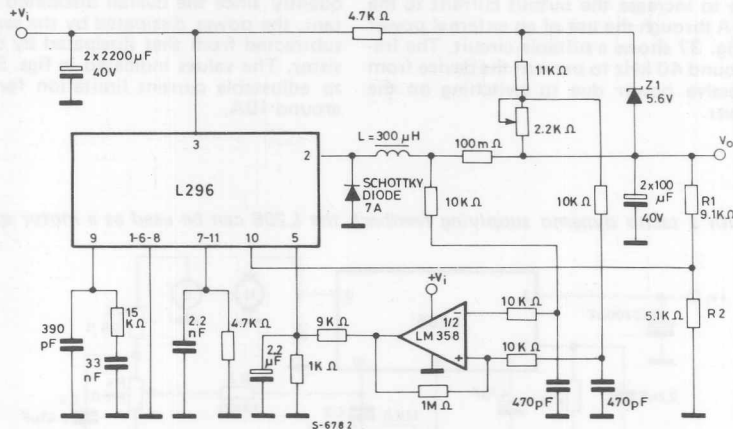
It is suggested that the diodes are fast types ($t_{rr} < 50$ nsec); should slower diodes be required some more turns have to be added to the auxiliary winding.

BATTERY CHARGER

When the device has to be used as current generator it is necessary to avoid the internal current limiter is operated. Fig. 34 shows the circuit realizing constant current limitation. In this way it is possible to obtain a 6V, 12V and 24V battery charger. For each of these voltages a max. current of 4A is avail-

able, which is large enough for batteries up to 40-45 Ah (for 12V type). With reference to the electric diagram through the 2K Ω potentiometer the max output current is set, while through the R₁ - R₂ output divider the voltage is set. (R₁ may be replaced by either a potentiometer or a 3 position switch, to directly obtain the three 6V, 12V and 24V voltages).

Fig. 34 - Battery charger circuit illustrating how the device is used to regulate the output current.



HIGHER INPUT VOLTAGE

Since a maximum input voltage of 46V (operating value) may be applied to the device the diagram shown in fig. 35 may be used when it is necessary to exceed this limit.

This system is particularly useful when operating at low output voltages. In this case a mean current I_{DC} which has a low value when compared to I_o is obtained. In fact, since $V_o = V_i (T_{ON}/T)$ and $V_o I_o = V_i I_{DC}$ (assuming the device has an ideal efficiency), it follows that $I_{DC} = I_o (T_{ON}/T)$.

Assuming to be:

$$V_o = 5V \quad I_o = 4A \quad \text{and} \quad V_3 \approx 37V,$$

it follows that:

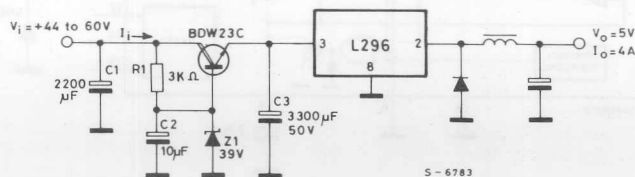
$$T_{ON}/T = V_o/V_i = \frac{5}{37} = 0.135$$

$$I_{DC} = 4 \times 0.135 = 0.54A.$$

With input voltage 50V and $I_o = 4A$, the external transistor dissipates about 7W. High good efficiency is still achieved, around 74%; in the real case, considering also the device losses, an efficiency around 62% is achieved.

During output short circuits the external transistor is not overloaded because in this condition I_{DC} reduces to values lower than 100mA. It is not possible to realize this application with series post-regulator because the efficiency would be unacceptably low.

Fig. 35 - The maximum input voltage can be raised above 46V by adding a transistor as shown here.



MOTOR CONTROL

The L296 is also suitable for use in motor controls applications. Fig. 36 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

HIGHER CURRENT REGULATORS

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Fig. 37 shows a suitable circuit. The frequency is around 40 kHz to prevent the device from losing excessive power due to switching on the external power.

The circuits shown in fig. 38 and fig. 39 show how current limitation may be realized in two different ways: through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat} ; when the resistor is connected in series to the collector V_{CE} is reduced; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor. The values indicated in figs. 38 and 39 realize adjustable current limitation for load currents around 10A.

Fig. 36 — With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller.

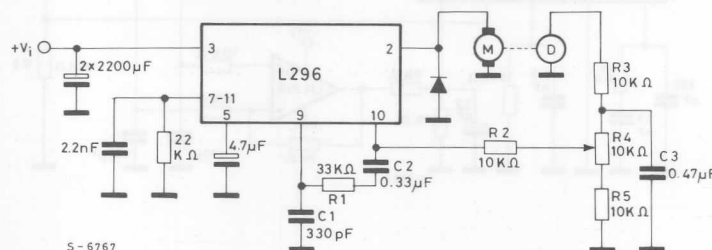


Fig. 37 — The output current may be increased by adding a power transistor as shown in this circuit.

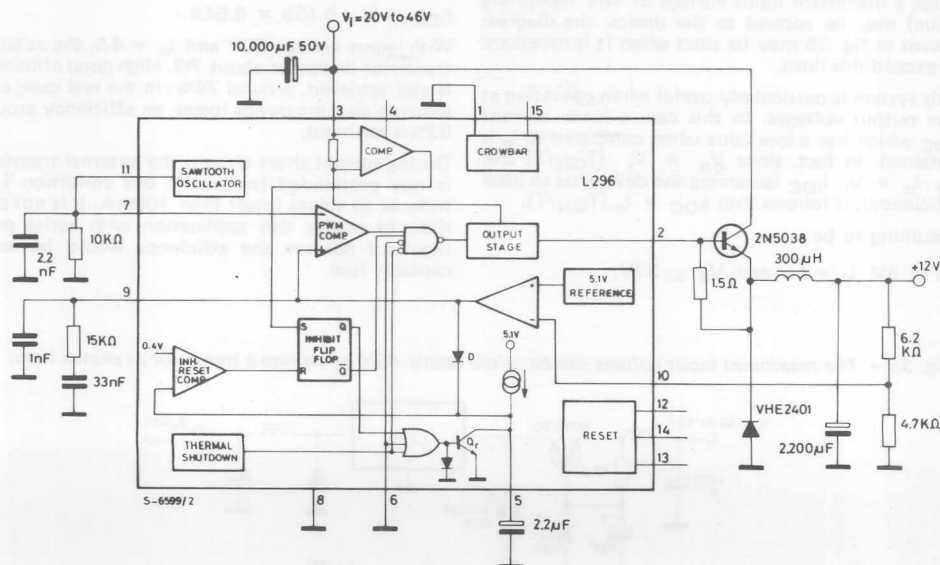


Fig. 38 — This circuit shows how current limiting for the external transistor is obtained with a sensing resistor.

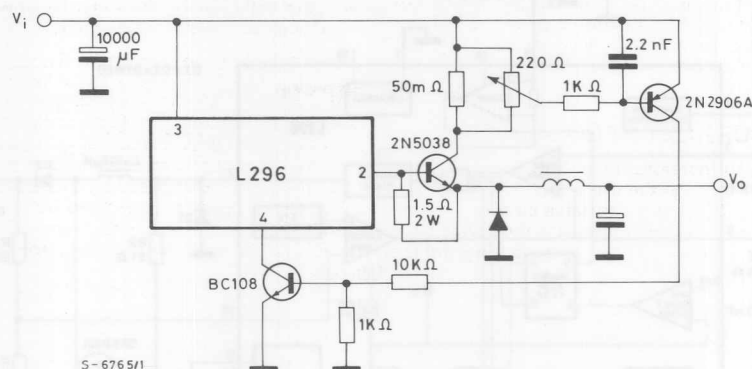
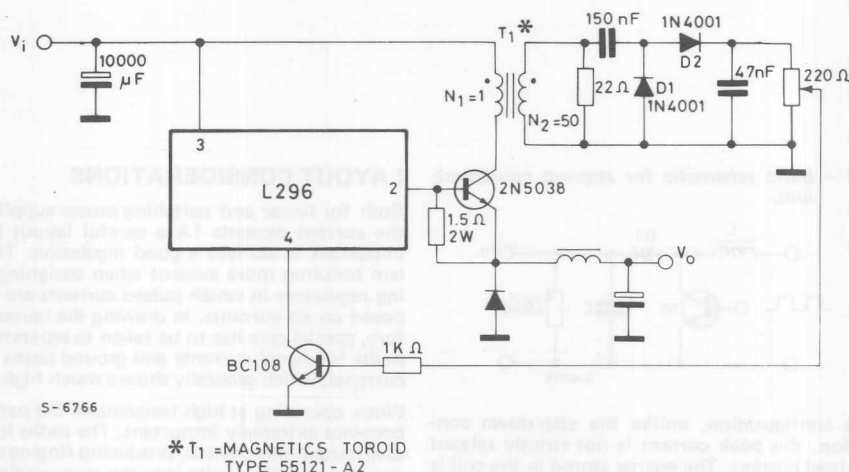


Fig. 39 — A small transformer is used in this example for current limiting.



STEP-UP CONVERTER

With the L296 it is also easy to realize a step-up converter, by using a MOS power transistor. Fig. 40 shows the electric diagram of the step-up converter. The frequency is 100 kHz, operation is in discontinuous mode and the device internal current limiter is used. Therefore no other external protection is required.

The input voltage could be a 12V car battery, from which an output voltage of 35V may be obtained. Lower output voltage values may be obtained by reducing the value of R7.

DESCRIPTION OF OPERATION

Fig. 41 shows the diagram of the circuit realizing the step-up configuration.

When the transistor Q1 is ON, the inductance L charges itself with a current given by:

$$i_L = \frac{V_i}{L} t$$

The peak current in the coil is:

$$I_{\text{peak}} = \frac{V_i}{L} T_{\text{ON}}$$

Fig. 40 — A step-up converter using a power MOS transistor.

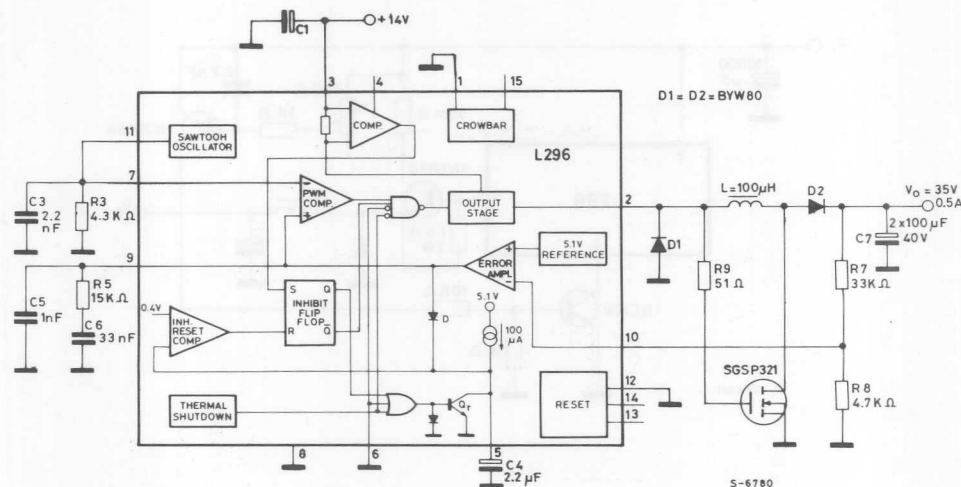
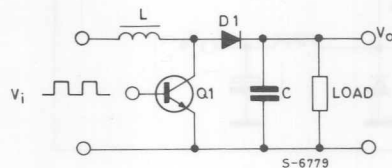


Fig. 41 — Basic schematic for step-up configurations.



In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is successively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used:

$$\frac{1}{2} L I_{\text{peak}}^2 = V_o I_o T$$

$$I_o = \frac{L I_{\text{peak}}^2}{2 V_o T} = \frac{V_i^2 T_{\text{ON}}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertainties when the current limitation operates. The electric diagram is shown in fig. 42.

LAYOUT CONSIDERATIONS

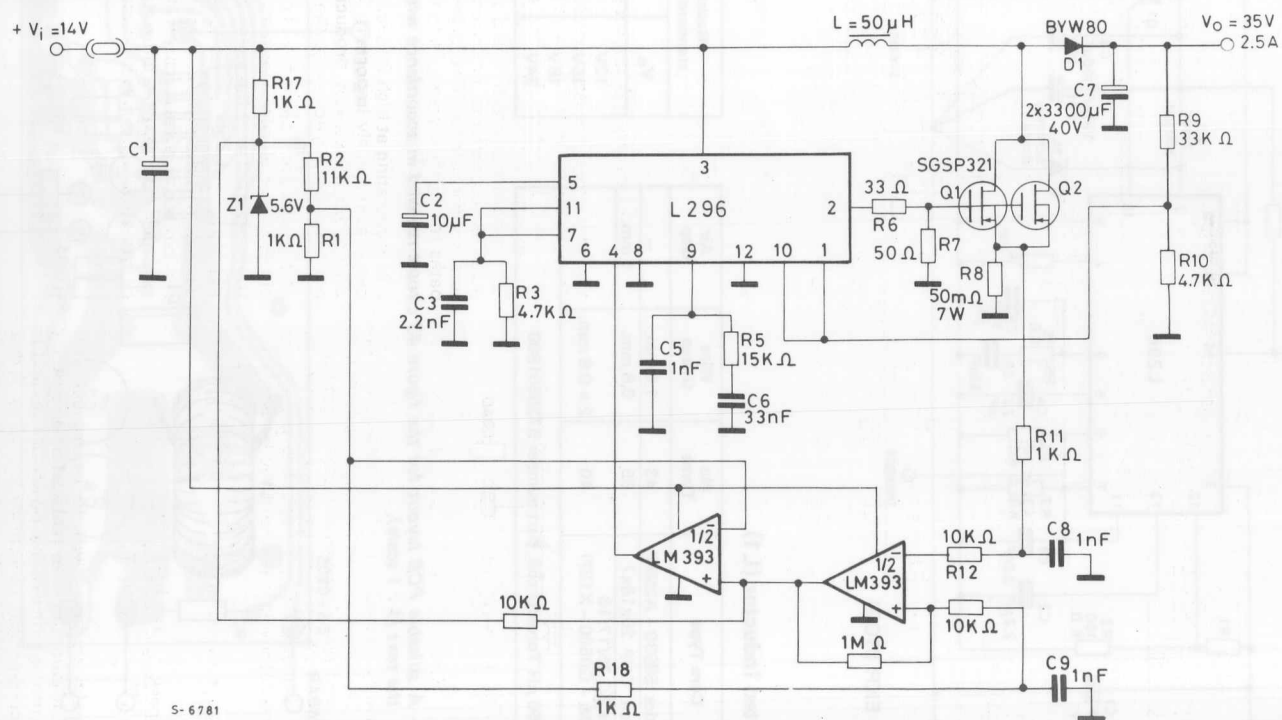
Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path length becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin 2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Fig. 43 and fig. 44 respectively show the electric diagram and the associated layout which has been realized taking these problems into account. Greater care must be taken to follow these rules when two or more mutually synchronized devices are used.

Fig. 42 — High power step-up converter showing how the current limiting function is realized externally.



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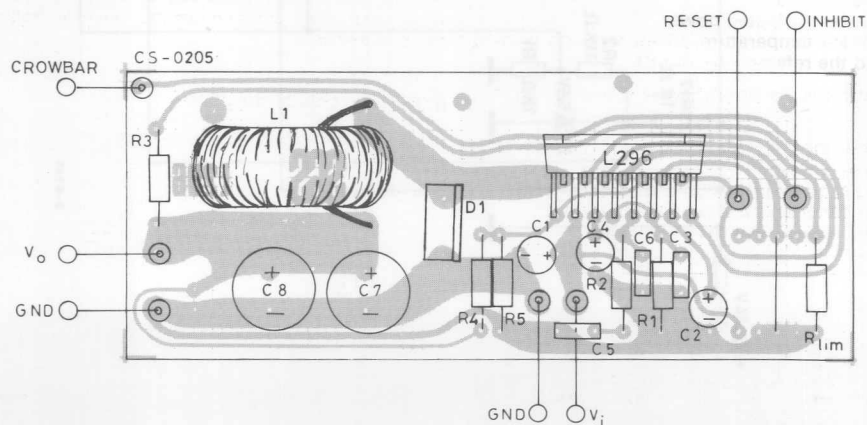


Suggested Inductor (L1)

VOGT 250 μ H Toroidal coil, part number 5730501800

V _o	R8	R7
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

Fig. 44 — A suitable PCB layout for the figure 43 circuit realized in accordance with the suggestions in the text (1 : 1 scale).



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150 °C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150 °C for long periods or of more than 170 °C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life; an increase of 10 °C can halve the device life. A well designed heatsink should keep the junction temperature between 90 °C and 110 °C. Fig. 45 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R_1 , R_2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 46).

Fig. 45

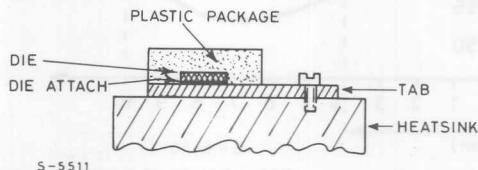
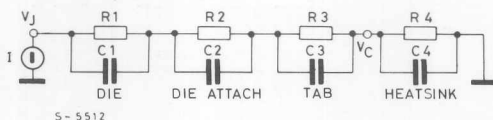


Fig. 46



C_1 , C_2 are the thermal capacitance (expressed in °C/W)

I is the dissipated power

V is the temperature difference with respect to the reference (ground)

This circuit can be simplified as shown in fig. 47, where:

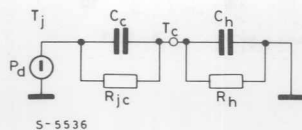
C_c is the thermal capacitance of the die plus that of the tab.

C_h is the thermal capacitance of the heatsink

R_{jc} is the junction case thermal resistance

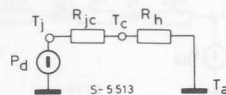
R_h is the heatsink thermal resistance

Fig. 47



But since the aim of this section is not that of studying the transistors, the circuit can be further reduced as shown in figure 48.

Fig. 48



If we now consider the ground potential as ambient temperature, we have:

$$T_j = T_a + (R_{jc} + R_h) P_d \quad a)$$

$$R_h = \frac{T_j - T_a - R_{jc} P_d}{P_d} \quad b)$$

$$T_c = T_a + R_h P_d \quad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5 °C/W; with silicone grease roughly 0.3 °C/W and with silicone grease plus a mica insulator about 0.4 °C/W. See fig. 49. In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the circuit shown in fig. 50. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult. This concept is better explained by the graph in fig. 51 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in fig. 51 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Fig. 49

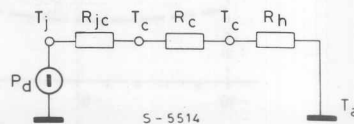


Fig. 50

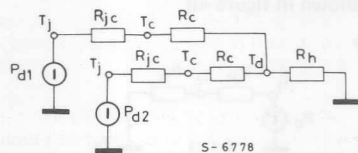


Fig. 52 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in application with two L296 synchronized.

Fig. 51

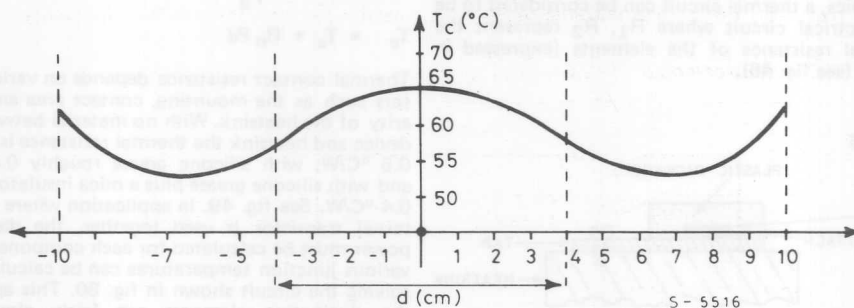
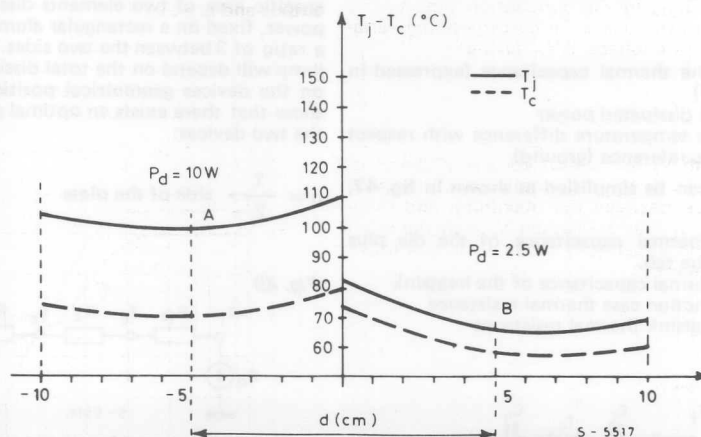


Fig. 52



APPENDIX A: CALCULATING SYSTEM STABILITY

This section is intended to help the designer in the calculation of the stability of the whole system.

Figure A1 shows the entire control system of the switching regulator.

The problem which arises immediately is the transfer function of the PWM block and output stage, which is non-linear. If this function can be considered linear the analysis is greatly simplified.

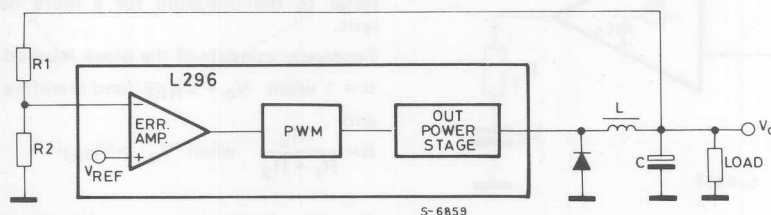
Since the circuit operates at a constant frequency and the internal logic is fairly fast, the error introduced by assuming that this function is linear is minimized. Factors which could contribute to the non-linearity are an excessive delay in the output power transistor, ringing and parasitic oscillations

generated in the power stage and non-linearity introduced by magnetic part.

In the case of the L296, in which the power transistor is internal and driven by well-controlled and efficient logic, the contribution to non-linearity is further reduced.

For the assumption of linearity to be valid the cut-off frequency of the LC filter must be much lower than the switching frequency. In fact, switching operation introduces singularities (poles) at roughly half the switching frequency. Consequently, as long as the LC filter is still dominant, its cut-off frequency must be at least an order of magnitude lower than the switching frequency. This condition is not, however, difficult to respect. The characteristics of LC filter affect the output voltage waveforms; is generally much less than an order of magnitude below the switching frequency.

Fig. A1 — The control loop of the switching regulator.



GAIN OF THE PWM BLOCK AND OUTPUT STAGE

The equation which links V_o to V_i is:

$$V_o = V_i \frac{T_{ON}}{T}$$

A variation ΔT_{ON} in the conduction time of the switching transistor causes a corresponding variation in the output voltage, ΔV_o , giving:

$$\frac{\Delta V_o}{\Delta T_{ON}} = \frac{V_i}{T}$$

Indicating with V_r the output voltage of the error amplifier, and with V_{ct} the amplitude of the ramp (the difference between the maximum and minimum values), T_{ON} is zero when V_r is at the minimum value and equal to T when V_r is at a maximum. Consequently:

$$\frac{\Delta T_{ON}}{\Delta V_r} = \frac{T}{V_{ct}}$$

The gain is given by:

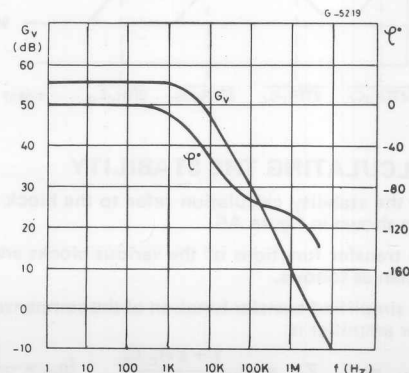
$$\frac{\Delta V_o}{\Delta V_r} = \frac{V_i}{V_{ct}}$$

Since V_{ct} is absolutely constant the gain of the PWM block is directly proportional to the supply voltage V_i .

ERROR AMPLIFIER

The error amplifier is a transconductance amplifier (it transforms a voltage variation at the input into a current variation at the output). It is used in open loop configuration inside the main control loop and its gain and frequency response are determined by a compensation network connected between its output and ground.

Fig. A2 — Open loop frequency and phase response of error amplifier.



In the application a series RC network is recommended which gives high system gain at low frequency — to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure A2 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7 kHz and a phase shift which reaches about -90° at frequencies around 1 MHz.

The introduction of a series network $R_C C_C$ between the output and ground modifies the circuit as shown in figure A3.

Figure A4 shows the gain and phase curves of the compensated error amplifier.

Fig. A3 — Compensation network of the error amplifier.

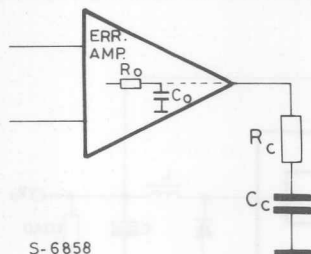
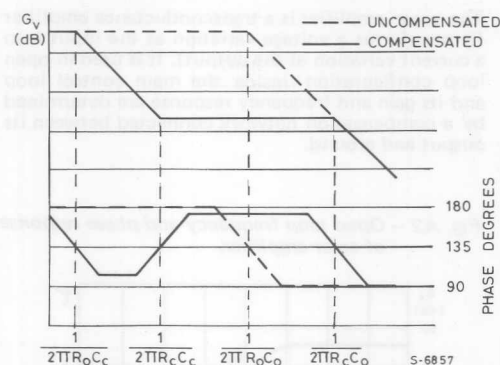


Fig. A4 — Bode plot showing gain and phase of compensated error amplifier.



CALCULATING THE STABILITY

For the stability calculation refer to the block diagram shown in figure A5.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is:

$$G_{EA} = g_m Z_c = g_m \frac{1 + s R_c C_c}{s C_c} \quad (g_m = \frac{1}{2500})$$

The DC gain must be considered equal to

$$A_o = g_m R_o$$

PWM block and output stage:

$$G_{PWM} = \frac{V_i}{V_{ct}}$$

LC FILTER:

$$G_{LC} = \frac{1 + s C \cdot ESR}{s^2 LC + s C ESR + 1}$$

where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Refer to the literature for a more detailed analysis.

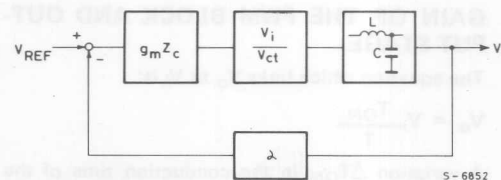
Feedback: consists of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R_2}{R_1 + R_2} \quad \text{when } V_o > V_{REF}$$

Fig. A5 — Block diagram used in stability calculation



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performance, once the frequency is fixed, are calculated with the following formulae:

$$L = \frac{(V_i - V_o) V_o}{V_i f \Delta I_L}$$

$$C = \frac{(V_i - V_o) V_o}{8 L f^2 \Delta V_o}$$

Since this filter introduces two poles at the angular frequency

$$\omega_o = \frac{1}{\sqrt{LC}}$$

we place the zero of the $R_c C_c$ network in the same place:

$$\omega_z = \frac{1}{R_c C_c}$$

Taking into account also the gain of the PWM block, the Bode plot of figure A6 is obtained.

The slope where the curve crosses the axis at 0 dB is about 40dB/decade therefore the circuit is unstable.

Taking into account now the zero introduced by the equivalent series resistance (ESR) of the output capacitor, we have further condition for dimensioning the $R_C C_C$ network. Knowing the ESR (which is supplied by the manufacturer for the quality components) we can determine the value of R_C so that the axis is crossed at 0dB with a single slope. The zero introduced by the ESR is at the angular frequency:

$$\omega_{zESR} = \frac{1}{ESR \cdot C}$$

The overall Bode diagram is therefore as shown in figure A7.

Fig. A6 – Bode plot of system taking filter and compensation network into account.

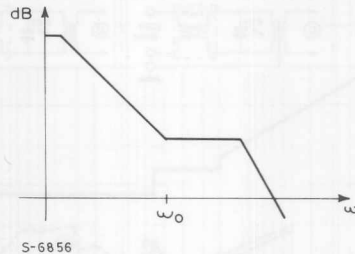
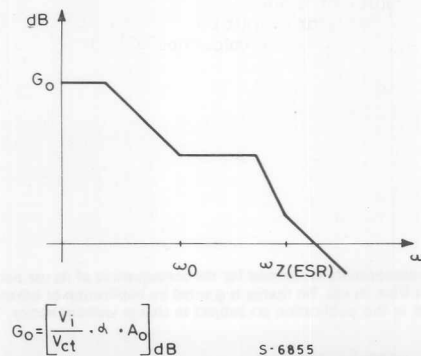


Fig. A7 – Bode plot of complete system taking into consideration the equivalent series resistance of the output capacitor.



DC GAIN AND LINE REGULATION

Indicating the open-loop gain of the error amplifier with A_0 , the overall open-loop gain of the system is:

$$A_t = A_0 \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}$$

When $V_o = V_{REF}$, the gain becomes:

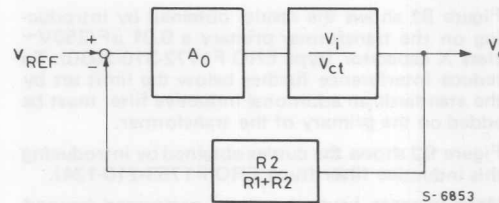
$$A_t = A_0 \frac{V_i}{V_{ct}}$$

Considering the block diagram of figure A8 and calculating the output variation ΔV_o caused by a variation of V_i , from the literature we obtain:

$$\frac{\Delta V_o}{V_o} = \frac{\frac{\Delta V_i}{V_i}}{\frac{A_0 V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}}$$

This expression is of general validity. In our case the percentage variation of the reference must be added by vector addition.

Fig. A8 – Block diagram for calculation of line regulation.



APPENDIX B: REDUCING INTERFERENCE

The main disadvantage of the switching technique is the generation of interference which can reach levels which cause malfunctions and interfere with other equipment.

For each application it is therefore necessary to study specific means to reduce this interference within the limits allowed by the appropriate standards.

Among the main sources of noise are the parasitic inductances and capacitances within the system which are charged and discharged fastly. Parasitic capacitances originate mainly between the device case and the heatsink, the windings of the inductor and the connection wires. Parasitic inductances are

generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasitic elements. The use of a diode with a fast reverse recovery time (t_{rr}) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences — RFI) to the levels permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allows the use of a filter with a relatively narrow bandwidth. For off-line switching regulators this filter is usually costly and bulky. In contrast, if the device is supplied from a 50/60 Hz transformer the RFI filter problem is greatly reduced.

Tests have been carried out at the laboratories of Roederstein to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see figs. B1 and B2) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with $V_o = 5.1V$ and $I_o = 4A$. The switching frequency is 100 kHz.

Figure B1 shows the results obtained by introducing on the transformer primary a 0.01 $\mu F/250V \sim$ class X capacitor (type ERO F1772-310-2030). To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure B2 shows the curves obtained by introducing this inductive filter (type ERO F1753-210-124).

Measurements have also been performed beyond 30 MHz; the maximum value measured is still well below the limit curve.

Fig. B1 — EMI measurements with a capacitor connected across the primary transformer with screen grounded (A) and floating (B)

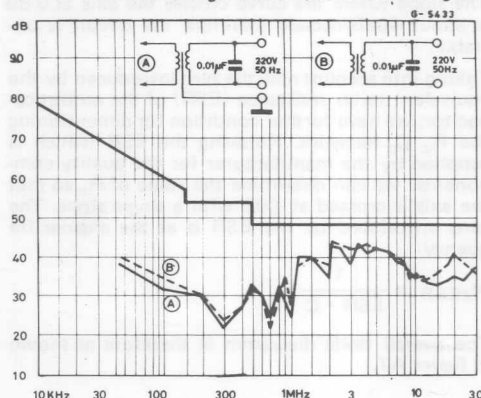
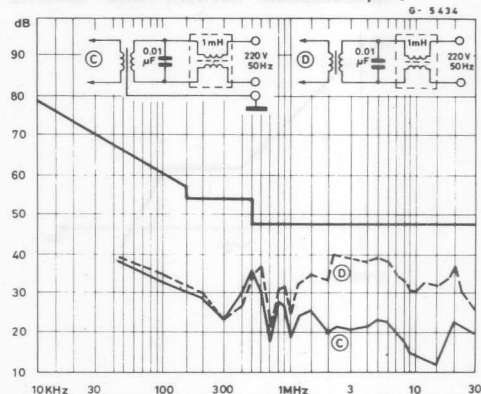


Fig. B2 — EMI results with the addition of an inductive filter on the mains input.



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TECHNICAL NOTE

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THE UC1524A INTEGRATED PWM CONTROL CIRCUIT PROVIDES NEW PERFORMANCE LEVELS FOR AN OLD STANDARD

INTRODUCTION

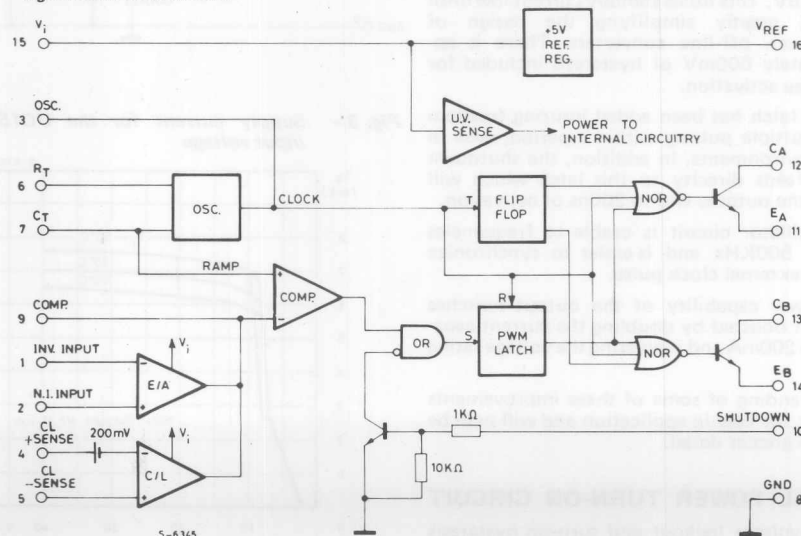
The application of IC technology to the switching power supply really began with the introduction of the SG1524 in 1976. This device was the first IC to implement all the control blocks necessary for a wide range of PWM power systems. Its straight-forward approach to the classic PWM architecture gave it wide acceptance, and it has become the most commonly used IC controller today.

Even though the 1524 has gained great acceptance and engineers have praised its versatile and easy to understand architecture, they have many times

curled the simplistic, or idealistic, ways its individual blocks were implemented. While one would assume, at first glance, that all control functions necessary for most power supply applications are contained within the 1524, in the real word of practical power systems, additional circuitry is required to interface with the rest of the system, to protect against different types of fault conditions, to adjust for inaccuracies, or to improve control during power sequencing.

Although in the intervening years, many new IC control chips have been introduced which offer certain specialized advantages, it was found that

Fig. 1 - The UC1524A block diagram follows the same architecture as the SG1524 but with several significant differences.



design engineers still preferred the 1524 for its wide versatility and generalized architecture. From this understanding, it became apparent that a new design, which would improve many of the 1524's individual functions by making them more predictable and easier to apply, while retaining the same architecture, could be a winner. The result is the UC1524A.

THE UC1524A PWM CONTROLLER

A design goal set for the UC1524A was that it not only retain the same architecture but keep the same pin configuration as the 1524 and function equal to or better than the 1524 in most existing applications. In this way, engineers who were familiar with the 1524 could easily understand and evaluate the UC1524A. Performance improvements had to be significant, particularly in reducing the need for discrete support circuitry, so there would be cost advantage in using the UC1524A in new design. The block diagram of the UC1524A is shown in Figure 1 which, by intent, appears very similar to that of the older 1524.

The list of the improvements, however, is considerable and includes the following:

1. The 5V reference is now internally trimmed to $\pm 1\%$ accuracy, eliminating the need for potentiometer adjustments.
2. The error amplifier's input range now extends beyond 5V, eliminating the need for a pair of dividers and their attendant tolerances.
3. A high-gain, wide-band, current sense amplifier has been included which is useful for either linear or pulse-by-pulse current limiting in the ground or power supply output lines.
4. An under-voltage lockout circuit has been added which disables all the internal circuitry except the reference until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low-power, off-line converters. There is approximately 600mV of hysteresis included for jitter-free activation.
5. A PWM latch has been added insuring freedom from multiple pulsing within a period, even in noisy environments. In addition, the shutdown circuit feeds directly to this latch which will disable the outputs within 200ns of activation.
6. The oscillator circuit is usable to frequencies beyond 500KHz and is easier to synchronize with an external clock pulse.
7. The power capability of the output switches has been boosted by doubling the current capability to 200mA and increasing the voltage rating to 60V.

An understanding of some of these improvements is necessary for ease in application and will now be discussed in greater detail.

INTERNAL POWER TURN-ON CIRCUIT

The under-voltage lockout and turn-on hysteresis

circuit is shown in Figure 2. This circuit requires approximately 2V for activation; but, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_i rises above 2V, R_2 begins to conduct saturating Q_3 and holding the base of Q_5 too low to allow any of the current sources to conduct. The current through R_4 flows through Q_3 and R_3 , developing a 600mV drop across R_3 when V_{REF} reaches 5V. At this level, the only current flowing is that used by the reference regulator and R_2 and R_4 , a total of approximately 2.5mA at turn-on threshold.

When the input voltage reaches approximately 8V, diode Z begins to conduct turning on Q_2 which turns off Q_3 and allows the current sources to activate. Since the current through Q_2 is much less than through Q_3 , the voltage across R_3 drops, providing positive feedback. This gives about 600mV of hysteresis. This circuit, of course, works in reverse at turn off, insuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 3 shows the relationship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with boot-strapped operation after turn on.

Fig. 2 — The under-voltage lockout and power turn-on circuitry within the UC1524A

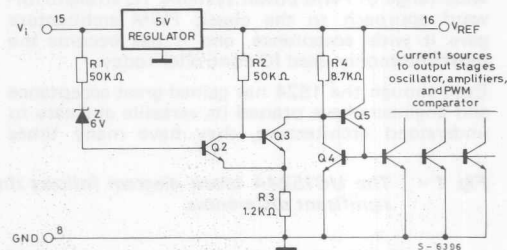


Fig. 3 — Supply current for the UC1524A vs. input voltage

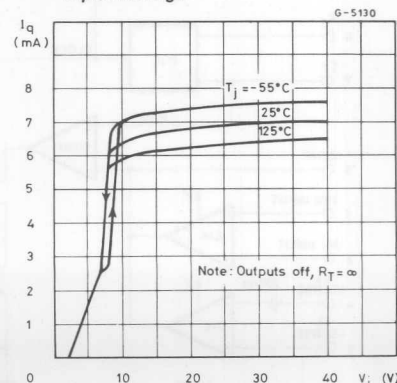
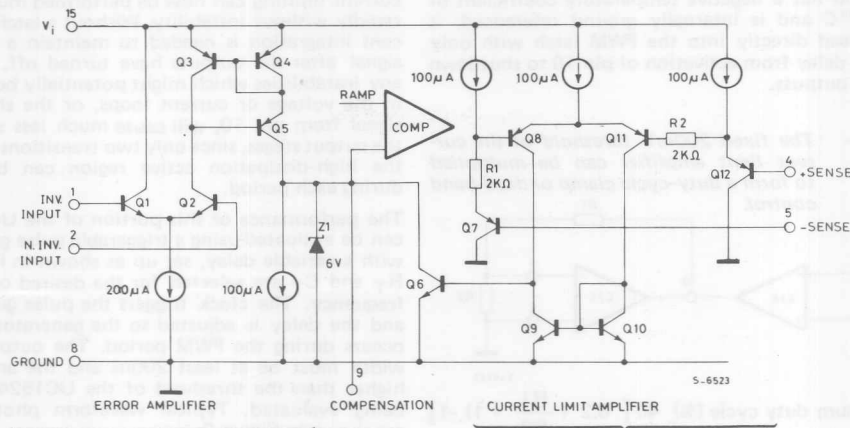


Fig. 4 - Voltage and current sensing amplifiers have a common output at the input to the PWM comparator.



A NEW CURRENT LIMIT AMPLIFIER

Since the outputs of the current limit amplifier and the voltage-sensing error amplifier are summed at the PWM comparator input, they should be examined together as shown in Figure 4.

Since the error amplifier, consisting of transistors Q_1 through Q_5 must have the lowest priority in controlling the PWM, its output must be easily overruled by current faults or other programming functions, such as soft-start, which would hold pin 9 low. Therefore, a transconductance amplifier similar to that used in the earlier 1524 was again applied to the 1524 with one exception: it is now powered by V_1 instead of V_{REF} , so that the input common-mode range extends to within 2V of either rail. Zener diode, Z_1 , is used on the output to keep the input level to the PWM comparator below 6 volts.

The error amplifier's output can be considered a $100\mu A$ current source or sink ($0 - 200\mu A$ source with $100\mu A$ constant sink). When the current limit circuit activates, Q_6 turns on and can easily pull down pin 9 even though the error amplifier would nominally be calling for a high output at this point.

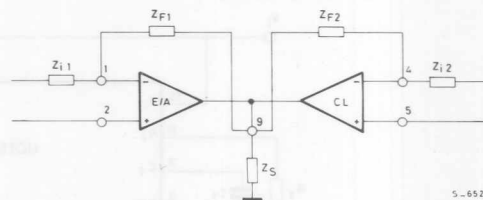
The current limit circuit consists of Q_6 through Q_{12} . Its differential PNP input stage gives it a common mode range extending from 300mV below ground to within -2V of V_1 . Its threshold or offset, of 200mV is established by the $100\mu A$ current source through R_1 , with R_2 added to null out the effect of any base current from Q_8 .

This current sensing block within the UC1524A can actually be used either as a linear amplifier or as a comparator. The open loop small-signal gain is approximately 80dB while its transition delay with 10% overdrive is 600ns. This can be decreased substantially with additional overdrive. Use of the current sensing block as a comparator is usually

preferred from a systems standpoint, since it does not have to be compensated and pin 9 can be dedicated solely to error amplifier compensation. Under this condition, a current signal over the threshold level will pull pin 9 low, terminating the output signal. Recovery is determined by the $100\mu A$ pull-up current from the error amplifier in conjunction with any capacitance which may be present on pin 9.

When the current limit circuit is used as a linear amplifier, stabilization is performed by feedback to the inverting input (pin 4) or by capacitance from pin 9 to ground as shown in Figure 5.

Fig. 5 - Various compensation options which are possible when both amplifiers are operated in the linear mode.

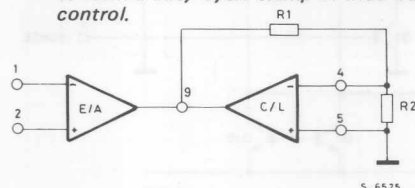


An additional feature of this circuit is its capability to perform as a duty-cycle limiting circuit in the configuration shown in Figure 6. If R_1 is made $100K\Omega$, there will be minimal effect upon the error amplifier gain.

In current limiting, to achieve the fastest responding pulse-by-pulse control, consideration should be given to the use of the shutdown terminal on pin

10. While the input threshold of this circuit is not as accurately controlled as the current limit amplifier and has a negative temperature coefficient of $-2\text{mV}/^\circ\text{C}$ and is internally ground referenced; it does feed directly into the PWM latch with only 200ns delay from activation of pin 10 to shutdown of the outputs.

Fig. 6 - The fixed 200mV threshold of the current limit amplifier can be multiplied to form a duty-cycle clamp or dead-band control.



$$\text{Maximum duty cycle (\%)} = 40 \left[0.2 \left(\frac{R1}{R2} + 1 \right) - 1 \right]$$

PWM COMPARATOR AND LATCH

The PWM latch insures only a single pulse is allowed to reach the appropriate output stage within each period. The latch is reset with the oscillator clock pulse which also serves to black the outputs. Thus, although the latch is reset at the start of the oscillator clock pulse, it is the termination of the clock pulse which initiates output conduction. The output then stays on until the latch is set, either by a signal from the PWM comparator or from a shutdown command from pin 10. Once the latch is set, it will hold the output off for the duration of the period.

These are several significant advantages to this circuit. First, the latch completely eliminates multiple outputs of the PWM comparator because of

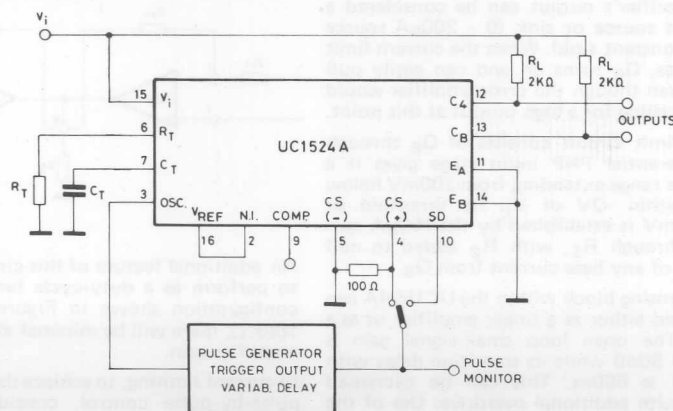
noise or ringing on the output of the error amplifier causing multiple crossing of the ramp signal. Second, current limiting can now be performed much more rapidly without instability. Without a latch, significant integration is needed to maintain a turn-off signal after the outputs have turned off. Finally, any instabilities which might potentially be present in the voltage or current loops, or the shutdown signal from pin 10, will cause much less stress on the output stages, since only two transitions through the high-dissipation active region can be made during each period.

The performance of this portion of the UC1524A can be evaluated using a triggerable pulse generator with a variable delay, set up as shown in Figure 7. R_T and C_T are selected for the desired operating frequency. The clock triggers the pulse generator, and the delay is adjusted so the generator output occurs during the PWM period. The output pulse width must be at least 200ns and the amplitude higher than the threshold of the UC1524A input being evaluated. Typical waveform photographs are shown in Figure 8.

HIGHER POWER OUTPUT SWITCHES

With the higher current and voltage rating of the UC1524A's output switches, significant economies can now be achieved in interfacing with higher power devices. For low power requirements, a broader range of applications may now be served by the 1524A itself without additional discrete output devices. Regardless of the power supply requirement, more current and voltage from the UC1524A will ease the design tradeoffs. Even with higher current and voltage, the UC1524A offers fast response time. Each output stage contains an anti-saturation network to keep the output transistors out of hard saturation. Although this adds somewhat to the saturation voltage, it is more than offset by the benefits in reducing turn-off delay.

Fig. 7 - Evaluating the turn-off delays of the UC1524A with the aid of a triggerable pulse generator with variable delay.



Saturation voltage as a function of current is shown in Figure 9.

Since both collectors and emitters are available on the UC1524A's output transistors, many different coupling possibilities are offered. One useful configuration for enhanced turn-off is shown in Figure 10. The fast-rising signal appearing at the collector of the output transistor, Q_1 , is capacitively coupled to saturate an external transistor, Q_2 , greatly reducing the turn-off delay of Q_3 and allowing a much larger value to be selected for R_3 . Many variations of this circuit are possible depending upon the power devices to be driven and the voltage levels required.

Fig. 8 - Typical turn-off response from both the current sense and shutdown inputs.

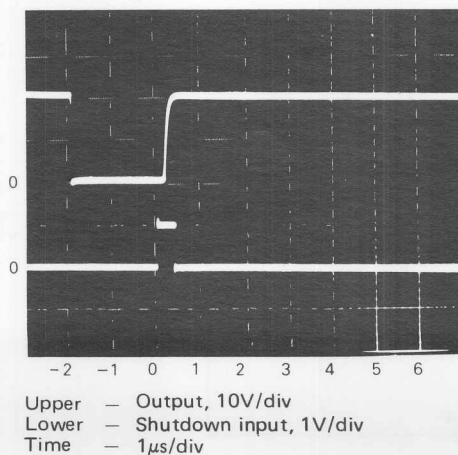
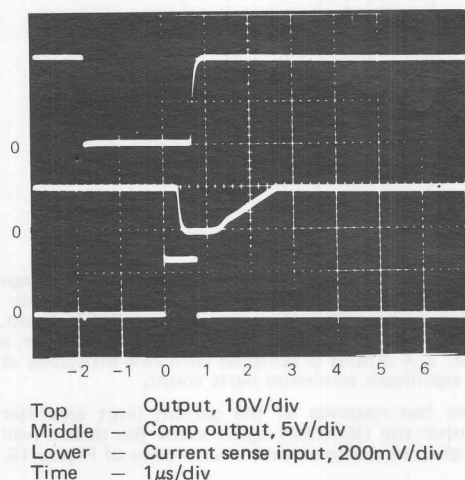


Fig. 9 - Output saturation characteristics for each of the UC1524A's outputs.

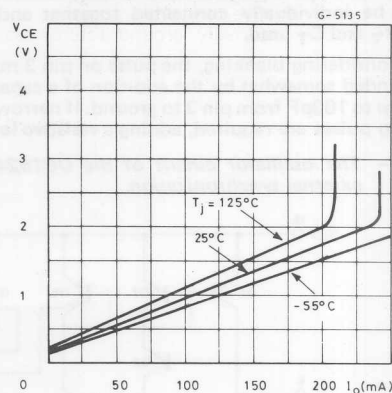
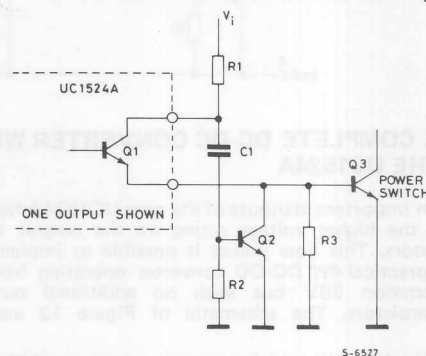


Fig. 10 - The addition of C_1 and Q_2 uses the collector signal of the UC1524A to generate an enhanced turn-off command for Q_3 .



FREQUENCY SYNCHRONIZATION

The oscillator circuit within the UC1524A, shown in Figure 11, has been improved over that of the 1524 with the addition of C_2 . Without this component a synchronizing pulse externally applied to pin 3 had to do all the work of discharging the timing capacitor through Q_4 and Q_5 . The simple addition of C_2 couples a positive pulse from pin 3 to the base of Q_{10} , momentarily reducing the threshold of comparator Q_8 - Q_9 and regeneratively triggering the oscillator into its discharge state. The circuit is now leading-edge triggered and narrow pulses can be used. This is a consideration when minimum dead time is required, since the outputs are blanked off as long as pin 3 is held high.

As with the 1524, synchronization to an external clock should be done with the $R_T C_T$ time constant set approximately 10 to 20% greater than that determined for the required clock frequency, taking into consideration the expected tolerances of the

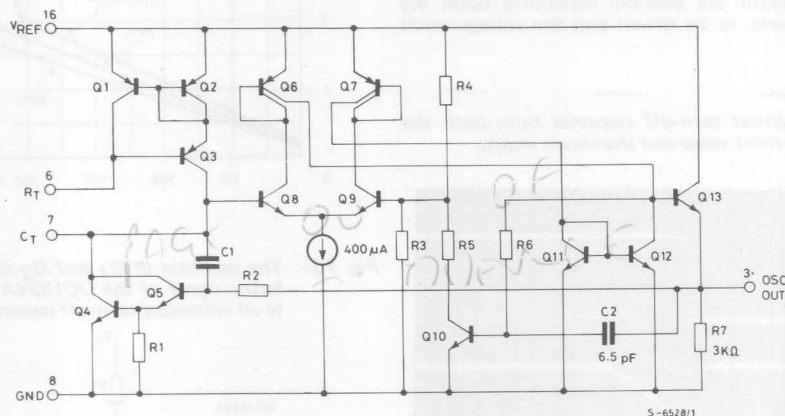
components. For synchronizing multiple UC1524A devices, all R_T , C_T , and OSC output terminals should be individually connected together and a single R_T and C_T used.

When considering blanking, the pulse on pin 3 may be extended somewhat by the addition of a capacitor of up to 100pF from pin 3 to ground. If narrower blanking pulses are required, adding a resistive load

from pin 3 to ground of 1K Ω minimum will reduce the pulse width.

The best way to guarantee a large dead time is still to use a diode to clamp the peak output from the error amplifier to a divider from V_{REF} . This technique is quite accurate due to the accuracy of V_{REF} and the 100 μ A fixed current available from the amplifier.

Fig. 11 - The oscillator circuit of the UC1524A allows both high frequency operation and ease of external synchronization.



A COMPLETE DC-DC CONVERTER WITH THE UC1524A

An important attribute of the new UC1524A family is the higher voltage rating on the output transistors. This now makes it possible to implement a practical 4W DC-DC converter operating from a common 28V bus with no additional output transistors. The schematic of Figure 12 uses a

push-pull configuration which imposes a voltage of twice the supply across the "OFF" transistor. This is now within the rating of the UC1524A and, thus, with a 28 : 7 turns ratio in the transformer, a 5V, ¾ A output is achieved with 78% efficiency at a significant minimum parts count.

The fast response of the current limit amplifier within the UC1524A again keeps the device well protected as shown in the waveforms of Figure 13.

Fig. 12 - With higher output voltage capability, the UC1524A can implement a complete 4W DC to DC converter with no additional switching transistors.

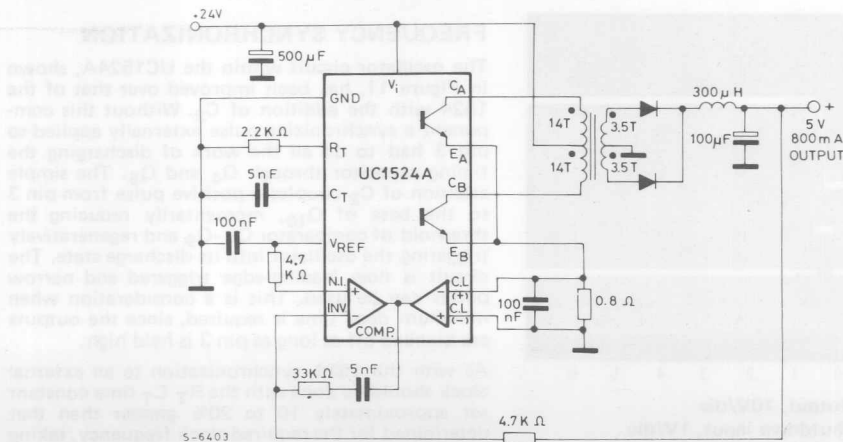
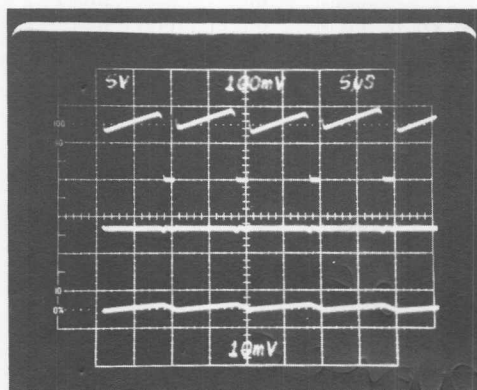
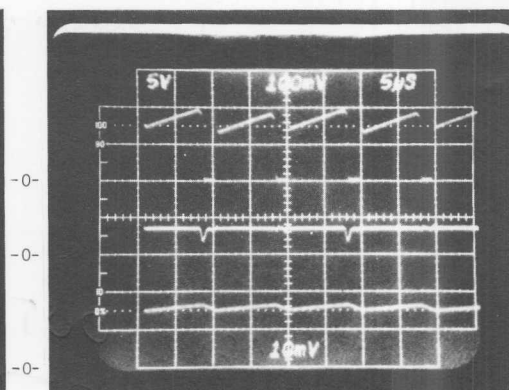


Fig. 13 - Operating waveforms for the PWM DC-DC converter (Fig. 12)

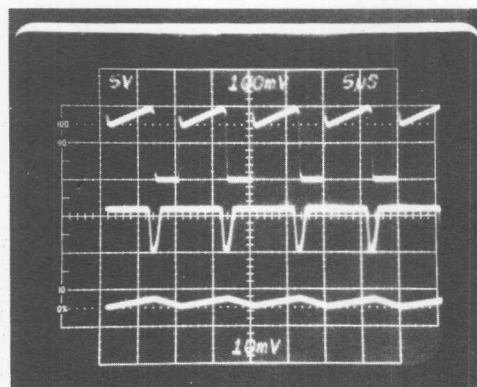
Upper trace = Primary current at 0.1A/division
 Middle trace = Pin 9 voltage at 5V/division
 Lower trace = Load current at 0.5A/division
 Time base = 5 μ s/division



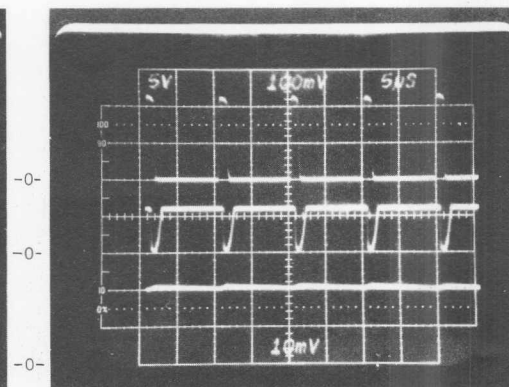
Circuit under normal load



Circuit at threshold of current limiting



Circuit under full current limit



Circuit under short circuit conditions

AN OFF-LINE FORWARD CONVERTER

For low to medium power application single-ended flyback or forward converter with all the control on the primary side of the isolation step-down transformer is usually the most economical solution. However there are two complications with this approach. The first is that although the control circuitry can easily be driven from a low-voltage winding on the power transformer, starting energy must be taken from the high-voltage rectified line where, at 170VDC, every 10mA represents a 1.7W loss. The second complication is in obtaining adequate regulation of the output while still meeting isolation requirements from output back to the line.

The 50W forward converter of Figure 14 offers innovative solutions to both these problems. In this circuit, the UC1524A provides all the control with its operating drive power coming from winding N_2 . The low-current start-up characteristics of the UC1524A allow starting energy to be developed in C_2 with only approximately 8mA required through R_1 .

The problem of isolated feedback control is solved in this application by sampling the 5V output level at the switching frequency by means of the 2N2222 transistors and transformer T_2 . With every switching cycle, the output voltage is transferred from N_1 to N_2 where it is peak detected to generate a primary-referenced signal to drive the PWM

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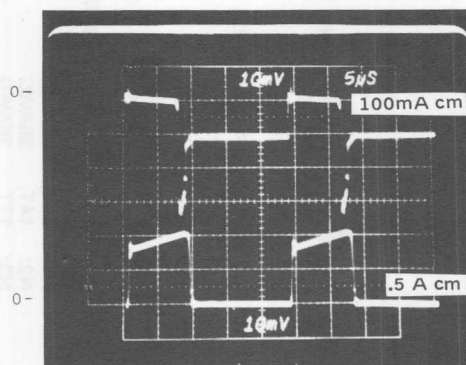
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maintaining input-output isolation.



Fig. 15 - Base current (upper trace) and collector current for the MJE13005 of fig. 14. The time base is $5\mu\text{s}$ per division



at Full Load (50W)

error amplifier. Diode D_2 is used to temperature compensate for the loss in the rectifier, D_1 and the net result is better than 1% regulation with the main added cost that of a very inexpensive signal transformer.

Some of the other features of this application include a duty-cycle clamp on the PWM formed by diode D_3 and the $10K - 1.5K$ divider from V_{REF} . This method of clamping is more effective with the UC1524A since the UV lockout keeps the outputs off until the reference, error amplifier, and oscillator are all operating within specification.

Drive for the MJE13005 high-voltage switch is accomplished by using the emitters of the UC1524A's output transistors for turn-on and the 2N2222 in conjunction with the $1\mu\text{fd}$ base capacitor to provide a negative base voltage for rapid turn-off as described in Figure 10.

The resultant drive signal is shown in Figure 15. Operating at 40KHz, this regulator provides an isolated 50W of power with an efficiency of 83%, a high degree of regulation, and fast overload protection.

CONCLUSION

Although there are now many new integrated circuits from which to choose in attempting to build more cost-effective power supplies, it always helps to review well established ideas. In the case of the UC1524A, updating and improving an earlier product has resulted in a significant advancement providing greater performance and versatility while reducing system costs.

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INTRODUCTION

Although this device contained all the basic control elements required for switching regulator design, practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

In order to be able to take full advantage of the speed capabilities of power MOS, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000pF present in higher current units.

The development of a second-generation regulating PWM IC, the SG1525A, and its complementary output version, the SG1527A, was a direct result of the desire to add more power supply elements to the control IC, as well as to optimize the interfacing of high current power devices.

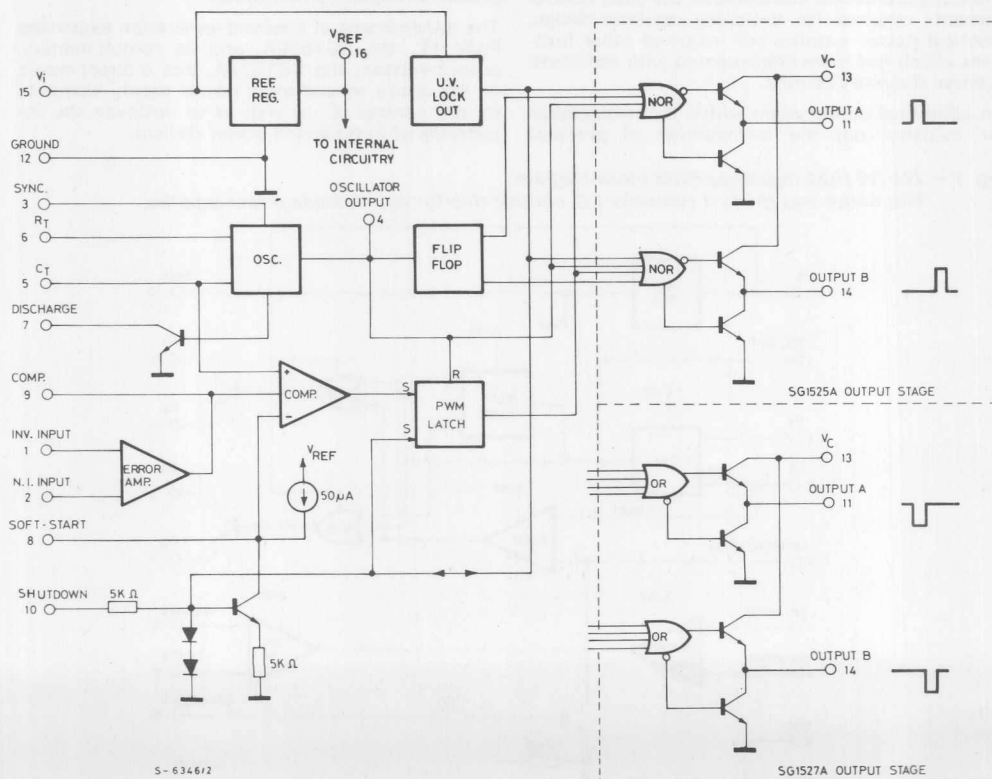
INTEGRATING MORE POWER SUPPLY FUNCTIONS

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in Figure 1, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated: 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the SG1525A is shown in Figure 2. Two general comments should be made relative to the overall block diagram. First, in optimizing the output stage for bi-directional, low im-

pedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the SG1525A device defined by an output configuration which is high during the ON pulse, and the SG1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q_4 (see Figure 3) for the SG1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

Fig. 2 — The SG1525A family represents a "second generation" of IC controllers.



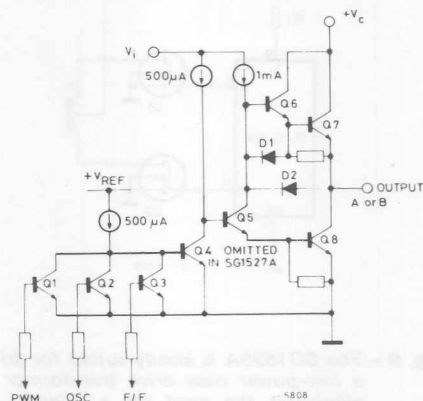
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"TOTEM-POLE" OUTPUT STAGE

One of the most significant benefits in using the SG1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the SG1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or Power MOS. The circuit schematic of one of the two output stages contained within the device is shown in Figure 3. This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C . Note that V_C is a separate terminal from the V_i supply to the rest of the device.

This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_i , the output cannot rise higher than approximately $1\frac{1}{2}$ volts below V_i .

Fig. 3 — One of two power output stages contained within the SG1525A which conduct alternately due to the internal flip-flop.



During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100 ns. A typical current waveform at V_C is shown in Figure 4. This transient will normally be decoupled from the rest of the control power by a $0.1\mu\text{F}$ capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

The output saturation characteristics of this stage are shown in Figure 5. The source transistor, Q_7 is

a straight forward Darlington and its saturation voltage remains between 1 and 2V out to 400 mA under the assumption that $V_i \geq V_C$. The sink transistor, Q_8 , however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50 mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8 . With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

Fig. 4 — Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.

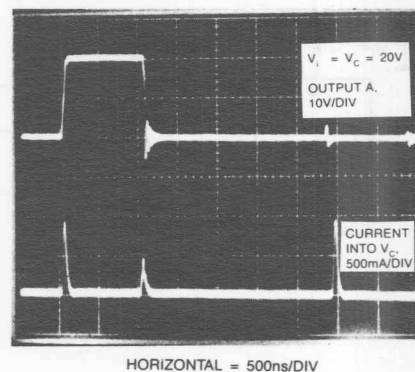
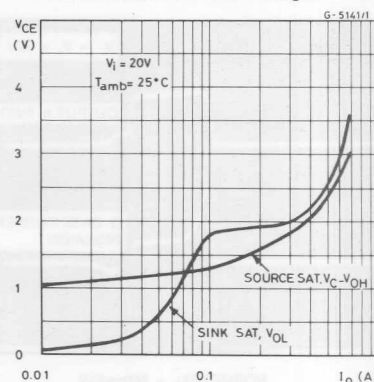


Fig. 5 — The output saturation characteristics of the SG1525A provide both high drive current and low hold-off voltage.



A typical output configuration for a push-pull bipolar transistor power stage is shown in Fig. 6. With a steady state base drive current from the SG1525A of 100mA, this stage should be able to switch 1 to 5A of transformer primary current, depending

upon the choice of transistors. The sum of R_1 and R_2 determine the maximum steady state output current of the SG1525A while their ratio defines the voltage across C_2 which, at turn off, becomes the reverse V_{BE} for Q_1 . With the values given, the output current and voltage waveforms are shown in Figure 7 for a one microsecond pulse. If power MOS are used for the output switches as shown in Figure 8, the interfacing circuitry can become even simpler with only a small series gate resistor potentially required to damp spurious oscillations within the power device.

Fig. 6 — A typical push-pull converter power stage using external bipolar power transistor switches.

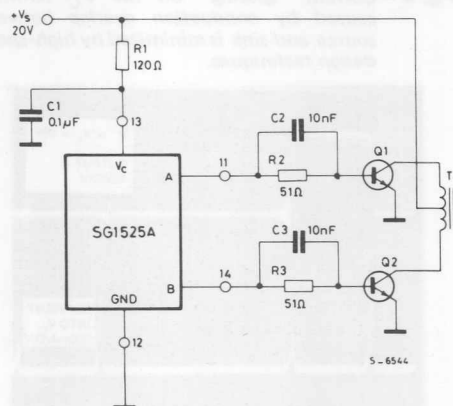
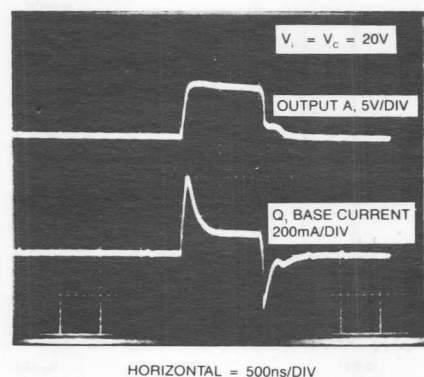


Fig. 7 — Base current waveforms (Figure 6 circuit) show the enhanced turn-on and turn-off current possible with the SG1525A.



Push-pull direct transformer drive is also particularly advantageous with SG1525A as shown in Figure 9. A version of this configuration is required for isolation when the control circuit is referenced

to the secondary side of an off-line power system, and to provide level shifting of drive signals for $\frac{1}{2}$ bridge and full bridge switching. The configuration of Figure 9 has a couple of important advantages. First, by connecting the drive transformer primary directly between the outputs of the SG1525A, no center-tap is needed and the full primary is driven with opposite polarities. Secondly, between each output pulse, both outputs are pulled to ground which effectively shorts the two ends of the primary winding together coupling a low-impedance turn-off signal to the switching transistors.

A useful single-ended configuration, typical of buck regulators, is shown in Figure 10. Here the SG1525A outputs are grounded and the PWM signal is taken from the V_C terminal which switches close to ground during each clock period as the internal source transistors are alternately sequenced.

Fig. 8 — Replacing bipolar transistors with power MOS provides even greater simplicity due to the low driving impedances of the SG1525A in each transition.

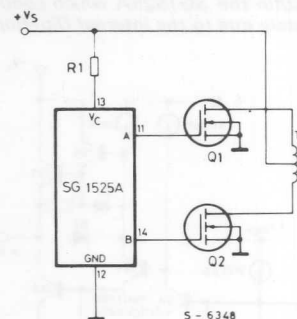
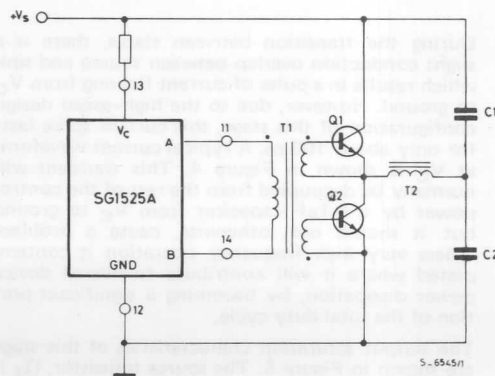


Fig. 9 — The SG1525A is ideally suited for driving a low-power base drive transformer and eliminates the need for a primary center-tap.



The diagram shows an inverting voltage-to-current converter circuit. An input voltage source $+V_s$ is connected to a resistor R_1 , which is in series with the base of a transistor Q_1 . The emitter of Q_1 is connected to ground (pin 12 of the SG1525A). The collector of Q_1 is connected to a resistor R_2 , which is in series with the output of the SG1525A (pin 11, labeled A). The output of the SG1525A is also connected to an output filter. The SG1525A is shown as a central component with pins 11 (A), 14 (B), and 12 (GND). The circuit is labeled S-6417/1.

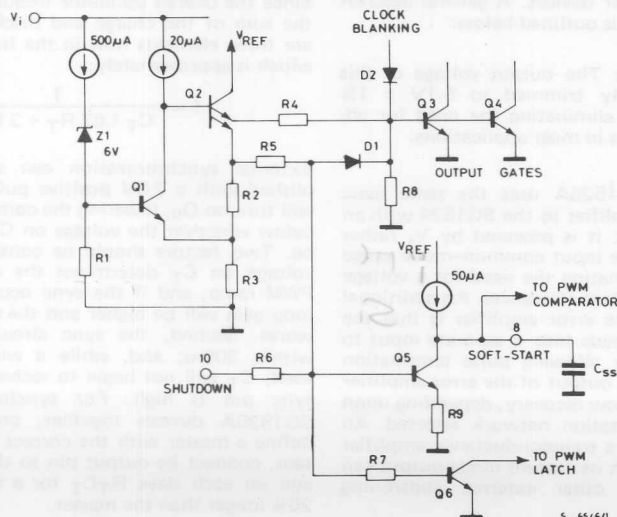
Although the advantages of the SG1525A's output stage will often be reason enough for its selection, there are several other important and useful features incorporated within this product. One problem previously overlooked in PWM circuits is keeping the output under control as the supply voltage is turned on and off. Undefined states, particularly the possibility of turning on an output before the oscillator is running, can be quite awkward, if not catastrophic. To prevent this, the SG1525A has incorporated an under-voltage lockout circuit which effectively clamps the outputs to the off state with as little as 2½V of supply

voltage which is less than the voltage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8V insuring that all the remaining SG1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5V. There is about 500mV of hysteresis built in to eliminate clamp oscillation at threshold.

Another important aspect of power sequencing is restraining the outputs from immediately commanding a 100% duty cycle when they are activated. This is accomplished by a slow turn on (soft-start) which is defined by an internal 50 μA current source in conjunction with an externally applied capacitor. The details of this power sequencing system are shown in Figure 11.

Q_3 and Q_4 are the output gates normally driven by the oscillator through D_2 to provide output blanking between pulses. (One of these transistors is shown as Q_2 in Figure 3). At low supply voltages, Q_2 conducts with base drive from the $20\mu A$ current source. Q_2 provides three functions. First, current through R_4 activates the output gates with minimum voltage drop. Second, current through R_5 activates the shutdown transistor Q_5 holding the soft-start capacitor, C_{SS} , discharged. Third, R_2 provides a small bucking voltage across R_3 for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q_1 , that transistor turns on. This turns off Q_2 , activating the outputs and allowing C_{SS} to begin to charge from the internal $50\text{ }\mu\text{A}$ current source. The time to reach approximately 50% duty cycle will be

[illegible]

POWER SUPPLY SHUTDOWN

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the SG1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to Figure 11, the base of Q_5 is turned on by a signal which is clamped to approximately 1.4V by the action of D_1 and the V_{BE} of gates Q_3 and Q_4 . This holds the outputs off and keeps C_{SS} discharged by Q_5 which, with R9, becomes a 100 μ A net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200ns through D_1 . Second, the PWM latch is set by Q_6 so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q_5 is activated commencing a 100 μ A discharge of C_{SS} . However, if the activation pulse on pin 10 has a duration shorter than $1/3$ of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS} , recycling soft-start.

Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

REGULATING PWM PERFORMANCE IMPROVEMENTS

The SG1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below:

Reference Regulator: The output voltage of this regulator is internally trimmed to 5.1V $\pm$ 1% during manufacture, eliminating the need for adjusting potentiometers in most applications.

Error Amplifier: SG1525A uses the same basic transconductance amplifier as the SG1524 with an important difference: it is powered by V_I rather than V_{REF} . Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM Comparator: The significant benefit of the SG1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The SG1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse current limiting by merely momentarily activating the shutdown circuitry within the SG1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

Oscillator: The functions of the oscillator within the SG1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple SG1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of Figure 12 for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8 , which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2 . The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D . As long as C_T is discharging, the clock output is high, blanking the outputs.

Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately:

$$f \approx \frac{1}{C_T (.07 R_T + 3 R_D)}$$

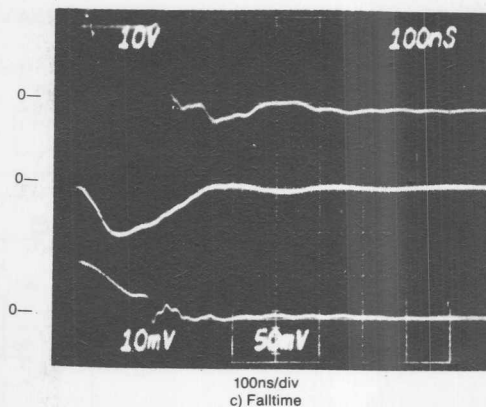
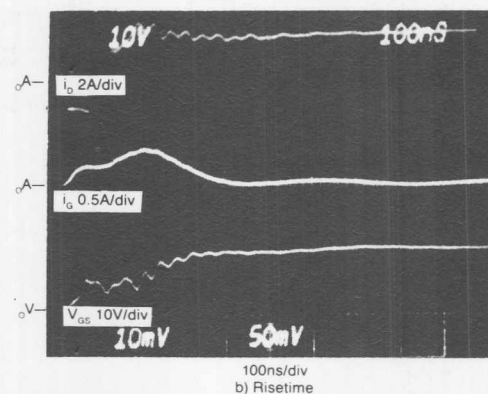
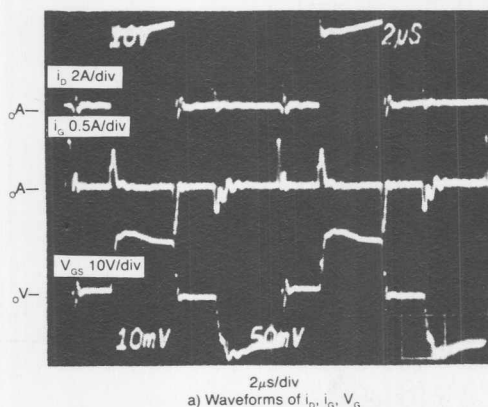
External synchronization can easily be accomplished with a 2.8V positive pulse at pin 3. This will turn on Q_9 , lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered: First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200ns; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple SG1525A devices together, one need only to define a master with the correct $R_T C_T$ time constant, connect its output pin to the slave sync pins, and set each slave $R_T C_T$ for a time constant 10-20% longer than the master.



Current limiting is provided by current transformer T3 in series with the primary of the power transformer T2. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the SG 1525A.

Waveforms of the converter are shown in the scope photos of Figure 16. Current rise and fall times are 20ns and 10ns.

Fig. 16 — Performance waveforms for the half-bridge, 500W, 100kHz converter with output current of 80A.



IMPROVED PERFORMANCE; LESS COMPLEXITY

Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the SG1525A provides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.

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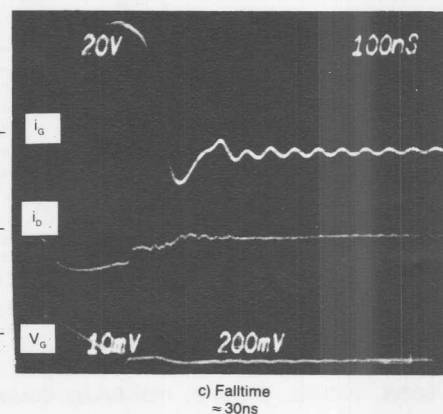
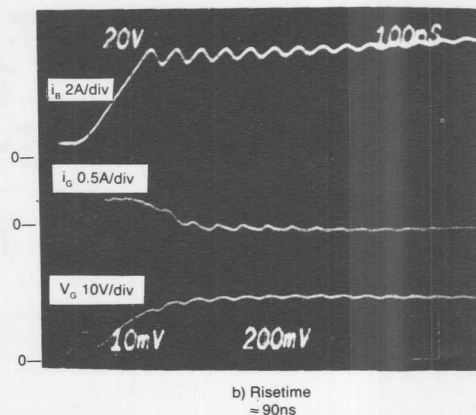
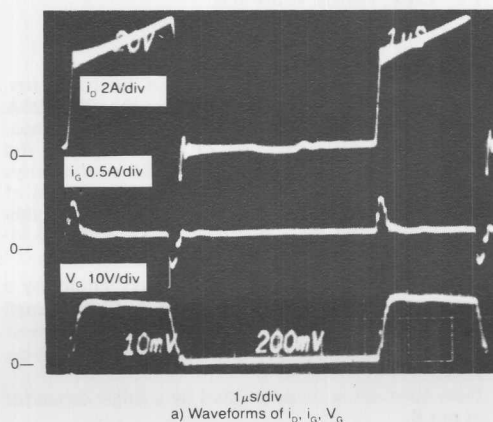
A 200 WATT, OFF-LINE, FORWARD CONVERTER

The ease of interfacing the SG1525A into a practical power supply system can be illustrated by the off-line, power converter shown in Figure 13. This 200W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a L123 or LM723. One other undefined block in Figure 13 is the auxiliary power supply which supplies the low voltage, low current bias supply for the SG1525A and the drive for Q_1 , the power switch. The choice of the SGSP479 power MOS for this switch keeps the total power requirements from the auxiliary supply at less than 1W; readily implemented with a small, line-driven transformer.

This converter is designed to operate at 150kHz which is accomplished by running the SG1525A at 300kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50%, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the 0.05 μ F capacitor on pin 9.

The totem-pole output of the SG1525A is used to advantage to drive Q_1 by providing a 400 mA peak current to charge and discharge the power MOS gate capacitance while keeping overall power dissipation low. Waveform photographs of this operation are shown in Figure 14.

Fig. 14 — Current and voltage waveforms for the 200W off-line forward converter with a SG1525A direct driven power MOS switch (operating frequency is 150kHz with output current equal to 40A).



When operating at full load, the efficiency of this converter is 73% with by far the greatest power losses occurring in the output rectifiers—even though Schottky devices have been selected.

Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during rise time due to Schottky rectifier capacitance.

Current limiting for this converter is provided by measuring the current in SGSP479 with the 0.1 Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the SG1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.

500W, 100kHz, Off-Line, Half-Bridge Converter:

- | | | | |
|----|---|----|--|
| T1 | Core: FerroX 486T250-3C8
Pri: 14T #22AWG
Sec (2): 7T #22AWG | T3 | Core: FerroX 486T250-3C8
Pri: 1T
Sec: 20T, C.T. #22AWG |
| T2 | Core: FerroX EC52-3C8 (EE)
Pri: 14T, 2 layers, 2 #16AWG in parallel
Sec (2): each 2T, C.T., copper strap 0.01" x 0.8" | T4 | 117V/220V, 25V, 0.15A, 50-60 Hz |
| | | L1 | Core: FerroX IF30-3C8
4 turns, 5 #12AWG in parallel |

The circuit shown in Figure 15 uses a pair of SGSP479 power MOS in a half-bridge configuration with the SG1525A chip referenced to the secondary side of the power transformer. The power MOS gates are driven directly from the control chip output through step down and isolation transformer T1. The SG1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of T1. This provides the fast, high current turn-on and turn-off pulses needed for the power MOS gates. In addition, the two ends of the primary windings are shorted to ground during deadtime.

which prevents accidental turn-on by transients. Note that the current supplied by the SG1525 outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T1 minimize ringing due to the power MOS gate capacitance and the inductance of T1 and lead inductance, particularly during deadtime.

Deadtime for the SG1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the power MOS have no storage time and a very short delay time.

Slow turn-on is accomplished by a single capacitor at pin 8.



TECHNICAL NOTE

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APPLYING THE UC1840 TO PROVIDE TOTAL CONTROL FOR LOW-COST, PRIMARY-REFERENCED SWITCHING POWER SYSTEMS

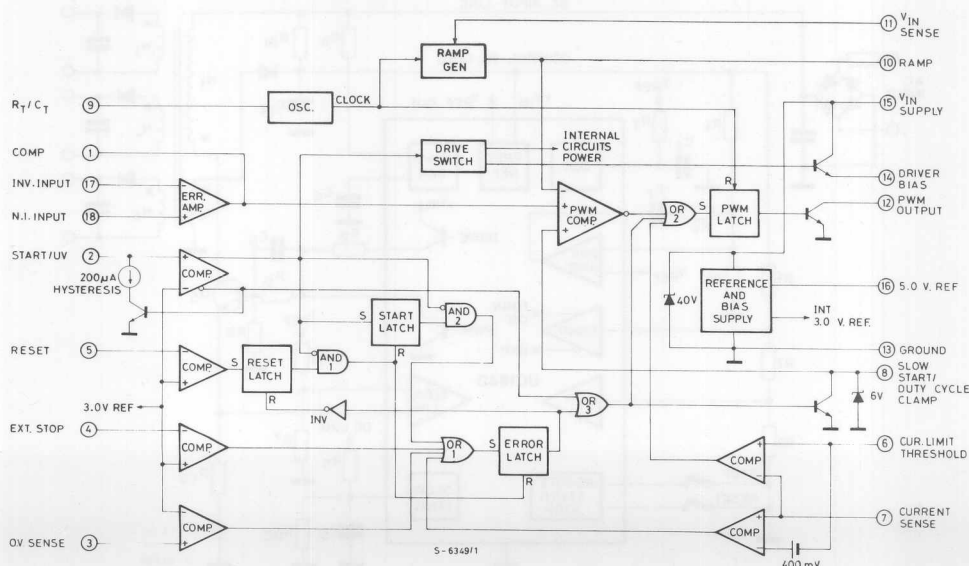
INTRODUCTION

There are many potential approaches to be considered in switch mode power supply design; however, the contradictory requirements of minimum cost and compatibility with ever more demanding line isolation specifications make primary control very attractive. Application of the UC1840 as a primary-side, off-line controller presents an

extremely cost-effective approach to supplying isolated power from a widely varying input line while maintaining a high degree of efficiency.

Primary control means referencing all of the control electronics along with the power switching device on the input line side of an isolation transformer. An obvious advantage to this approach is the simplified interface between the control and

Fig. 1 - The overall block diagram of the UC1840, an integrated circuit optimized for primary-side control of off-line switching power supplies.



power switch. This eliminates many of the transitions across the isolation boundary which significantly increase the cost of the magnetics portion of the power supply's budget.

There are two disadvantages to primary control: (1) operating or at least starting, the control electronics from the line voltage (typically 300 VDC), and (2) providing adequate regulation (which requires feedback from the secondary across the isolation boundary). The capability of the UC1840 Control IC to solve these problems while providing all of the regulating, sequencing, monitoring, and protection functions referenced to the primary side, makes this device very attractive.

THE UC1840 CONTROLLER

The overall block diagram of the UC1840, shown in Figure 1, includes the following features:

- (1) Fixed-frequency operation set by user-selected components.
- (2) A variable-slope ramp generator for constant volt-second operation providing open-loop line regulation and minimizing, or in some cases even eliminating, the need for feedback control.
- (3) A drive switch for low current start-up off the high-voltage line.
- (4) A precision reference generator with internal over-voltage protection.

(5) Complete under-voltage, over-voltage, and over-current protection including programmable shutdown and restart.

(6) A high-current, single-ended PWM output optimized for fast turn-off of an external power switch.

(7) Logic control for pulse-commandable or DC power sequencing.

For an understanding of how these individual blocks work together in a typical, medium-power flyback power supply, reference should be made to Figure 2 and the functional description which follows.

UC1840 FUNCTIONAL DESCRIPTION

Power sequencing

A simplified schematic of the UC1840's internal power turn-on circuitry is shown in Figure 3. The key elements of this function are: (1) the Driver Bias Switch, Q3, which keeps the loading on the control voltage line, V_C , to a minimum during start up; (2) the Under-voltage Comparator which also functions as a Start Threshold Detector with programmable hysteresis; and (3) an auxiliary, primary-referenced, low-voltage winding on the main power transformer which provides normal control power after turn-on. The sequence of events is as follows:

Fig. 2 - A fully protected, isolated flyback power supply can be implemented with the UC1840, a high-voltage power switch, the transformer, and a small handful of passive components.

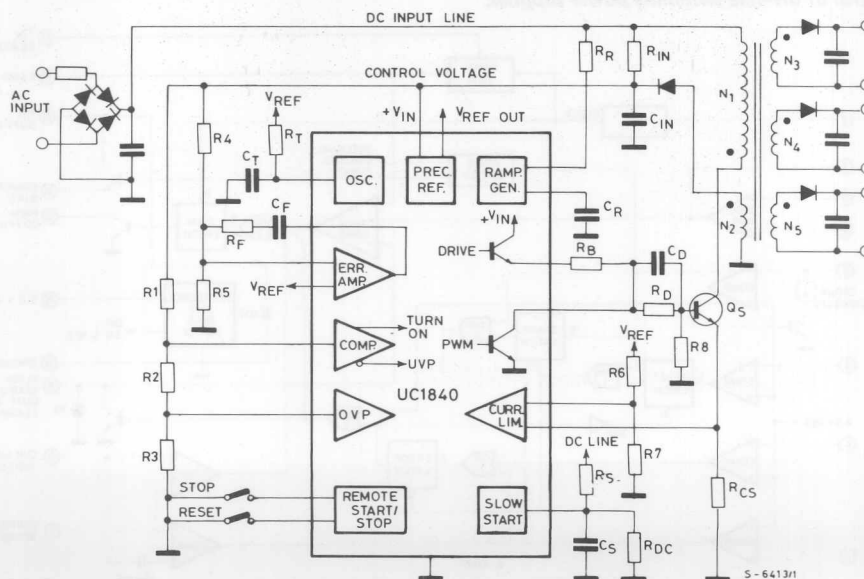
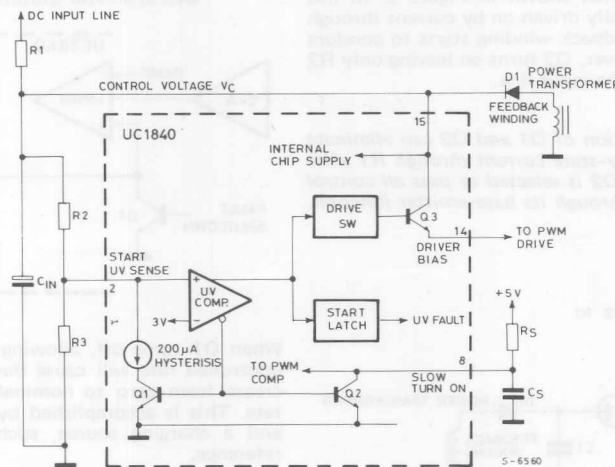


Fig. 3 - The UC1840's start circuitry requires low starting current from the DC input line with normal operating current supplied from a low-voltage feedback winding on the power transformer.



- (1) While the control voltage, V_C , is low enough so that the voltage on pin 2 is less than 3V, the Start/UV Comparator does the following:

- (a) A $200\mu\text{A}$ hysteresis current is flowing into pin 2 through Q1 causing an added drop across R2.
- (b) The drive switch is holding the Driver Bias transistor, Q3, OFF. This insures that the only current required through R1 is the start-up current of the UC1840, plus external dividers (R2, R3, R_S , etc.).
- (c) The Slow Turn-on transistor, Q2, is ON, holding pin 8 and C_S low.
- (d) The Start Latch keeps the under-voltage signal from being defined as a fault.

- (2) The start level is defined by:

$$V_C(\text{start}) = 3 \left(\frac{R_2 + R_3}{R_3} \right) + 0.2 R_2.$$

When V_C rises to this level, the Start/UV Comparator then does the following:

- (a) Turns off Q1, eliminating the $200\mu\text{A}$ hysteresis current. This allows the voltage on V_C to drop before reaching the under-voltage fault level defined by:

$$V_C(\text{U.V. fault}) = 3 \left(\frac{R_2 + R_3}{R_3} \right)$$

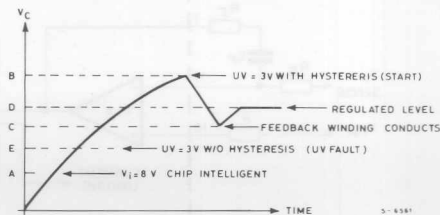
- (b) Sets the Start Latch to monitor for an under-voltage fault.
- (c) Activates Q3 providing Driver Bias to the power switch, pulling the added current out of C_{IN} .
- (d) Turns off Q2 allowing for programmed slow turn-on defined by R_S and C_S .

- (3) A normal start-up occurs with the control voltage, V_C , following the path shown in Figure 4. If the power supply does not start, V_C will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon the status of the Reset terminal as defined under Fault Sequencing. If start-up does not occur because of some fault in the Driver Bias line, V_C will continue to rise until the 40V zener across the reference circuit conducts. This will then clamp V_C to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of:

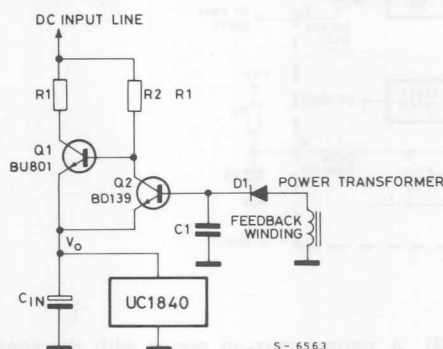
$$P_d = \frac{(V_{line} - V_C)^2}{R_1}$$

Fig. 4 - Under a normal turn-on, the supply voltage to the UC1840, V_C , would rise lightly loaded to the start level, fall under the turn-on load, and then regulate at some intermediate level.



If this loss is objectionable, it can be reduced more than an order of magnitude by the addition of a two-transistor switch shown in Figure 5. In this circuit, Q1 is initially driven on by current through R2. When the feedback winding starts to conduct through D1, however, Q2 turns on leaving only R2 conducting from the input line.

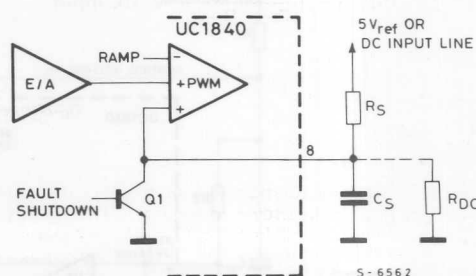
Fig. 5 - The addition of Q1 and Q2 can eliminate the steady-state current through R1 after turn-on. Q2 is selected to pass all control current through its base-emitter junction.



Slow turn-on circuit

The PWM comparator input connected to pin 8 accommodates several programming functions, shown in Figure 6. Since this comparator will only follow the lowest positive input, holding pin 8 low will effectively eliminate a PWM signal, regardless of the status of the Error Amplifier output. Prior to turn-on, and at all times when a fault has been sensed, Q1 is ON, holding pin 8 low.

Fig. 6 - Pin 8 on the UC1840 can be used for both slow turn-on and duty-cycle limiting as well as a PWM shutdown port.

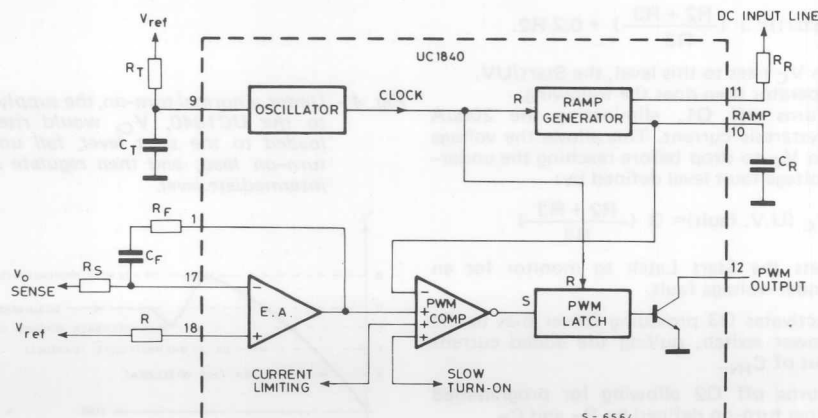


When Q1 turns off, allowing pin 8 to rise with a controlled rate will cause the output pulses to increase from zero to nominal widths at the same rate. This is accomplished by the addition of C_S and a charging source, such as R_S, to the 5V reference.

Note that where starting energy is stored in an input capacitor, the time for PWM turn-on must be less than the time required for the added Driver Bias load current to discharge the input capacitor to the under-voltage fault level. In other words, referring back to Figure 4, the slow turn-on must be faster than the time required for V_C to fall from level B to level E.

Another function of pin 8 is to establish a maximum duty cycle limit. This is achieved by clamping the voltage on pin 8 with a divider formed by adding R_{DC} to ground. If R_S is taken to the 5V reference, the clamp voltage will be fixed, which is desirable if the ramp slope is also fixed. If the ramp slope is varied with the input line — for constant volt-second operation — then the clamp voltage on pin 8 must also vary. This is readily accomplished

Fig. 7 - The pulse-width modulator within the UC1840 separates the ramp function from the fixed-frequency oscillator.



by connecting R_S to the DC input line. The divider voltage:

$$V_{\text{Pin 8}} = \left(\frac{R_{\text{DC}}}{R_S + R_{\text{DC}}} \right) V_{\text{DC input}}$$

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

PWM control

Pulse-Width Modulation within the UC1840 consists of the blocks shown in Figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

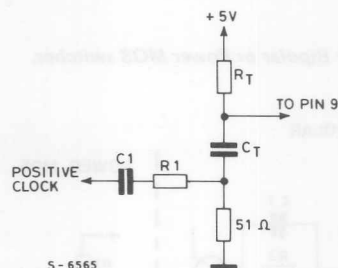
Oscillator

A constant clock frequency is established by connecting R_T from pin 9 to the 5V reference and C_T from pin 9 to ground. The frequency is approximated by:

$$f \approx \frac{1}{R_T C_T}$$

where the value of R_T can range from 1 k Ω to 100 k Ω and C_T from 300 pF to 0.1 μ F. The best temperature coefficients occur with C_T in the range of 1000 to 3000 pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of Figure 8, where R_1 and C_1 are selected to provide a 0.5V, 200 ns pulse across the 51 Ω resistor, and R_T and C_T define a frequency slightly lower than the synchronizing source.

Fig. 8 - Synchronization to an external time base can be accomplished by adding a 51 Ω resistor in series with C_T .

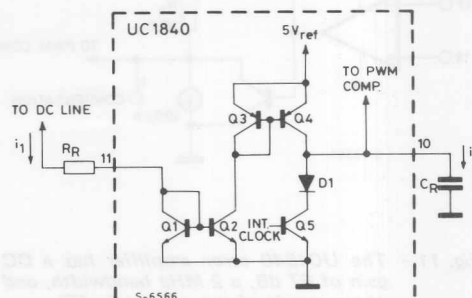


To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

Ramp generator

The ramp generator function of the UC1840 is shown in simplified form in Figure 9.

Fig. 9 - Current mirrors Q1-Q4 are used to make the ramp charging current i_2 , linearly proportional to the DC input line.



The NPN and PNP current mirrors provide a charging current to C_R of:

$$i_2 = i_1 = \frac{V_{\text{line}} - 0.7V}{R_R} \approx \frac{V_{\text{line}}}{R_R}$$

The current mirrors are useful over a current range of 1 μ A to 1 mA, but optimum tracking occurs between 30 μ A and 300 μ A. Since the voltage across Q1 is very small, i_2 accurately represents the input line voltage. The ramp slope, therefore, is:

$$\frac{dv}{dt} = \frac{V_{\text{line}}}{R_R C_R}$$

The peak voltage across C_R is clamped to approximately 4.2V while the valley, or low voltage, is determined by the on-voltage of the discharge network, D1 and Q5. This is typically 0.7V.

If line sensing is not required, R_R should be connected to the 5V reference for constant ramp slope.

Error amplifier

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in Figure 10.

The 1 k Ω output resistor, R_O , is used both for short circuit protection and to limit the peak output voltage to less than 4.0V so it cannot rise above the clamped ramp waveform. At sink currents less than 300 μ A, the low output level will be within 200mV of ground but it rises to 1V at higher current levels.

The input common mode range is from 1V to within 2V of the input supply voltage. V_{in} , and thus either input can be connected directly to the 5V reference.

Fig. 10 - The output of the error amplifier operates class A to $300\mu\text{A}$, but can source and sink more than 1 mA for fast response.

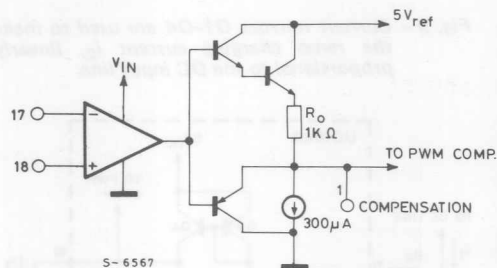
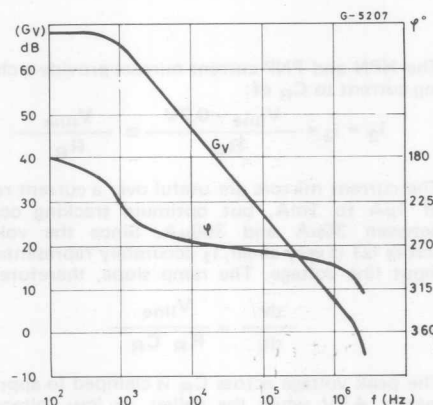


Fig. 11 - The UC1840 error amplifier has a DC gain of 67 dB, a 2 MHz bandwidth, and phase margin of approximately 45° .



The small signal, open-loop gain characteristics are shown in Figure 11. The amplifier is unity-gain stable and has a maximum slew rate of just under $1\text{V}/\mu\text{s}$.

PWM comparator and latch

This comparator (see Figure 7) generates the output pulse which starts at the termination of the clock pulse and ends when the ramp waveform crosses the lowest of the three positive inputs. The clock forms a blanking pulse which keeps the maximum duty cycle less than 100%. The PWM latch insures there will be only one pulse per period and eliminates oscillation at comparator cross-over.

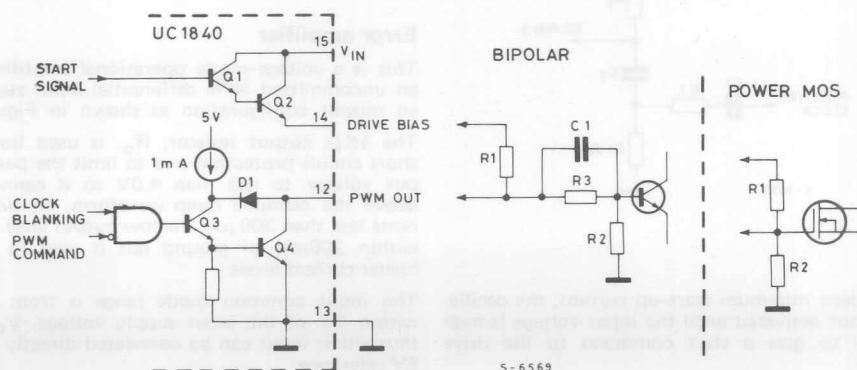
PWM output stage

In addition to the PWM output signal on pin 12, the UC1840 also includes an output gating, or arming function as Driver Bias on pin 14. Both functions should be considered together in interfacing to the external high-voltage power switch. These are illustrated in simplified form in Figure 12.

At very low input voltages ($V_{IN} < 3\text{V}$), both Q2 and Q4 are OFF. This may necessitate the use of R2, but its value can be high since it does not have to turn the output switch off. It merely holds it in the off state during the early portion of start-up.

Between $V_{IN} = 3\text{V}$ and the start threshold (pin 2 = 3V with hysteresis on), Q2 is OFF and Q4 is ON, clamping the power switch off with a low impedance. A start command (UV high) turns on Q2, applying ($V_{IN} - 2\text{V}$) to R1. This provides a source for power switch activation; however, since Q4 is still conducting, the current through R1 is shunted to ground and the power switch remains held off.

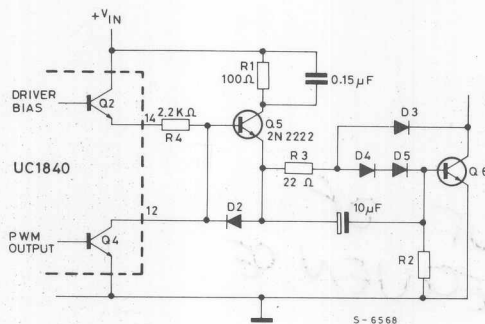
Fig. 12 - Interfacing the UC1840 PWM output stage to either Bipolar or Power MOS switches.



At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4 — narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several different ways to meet varying system requirements. One obvious application is when the use of a bipolar transistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

Fig. 13 – Adding Q5 as a switched, drive-boost transistor provides added base drive for Q6 while reducing the steady-state current through both Q2 and Q4.



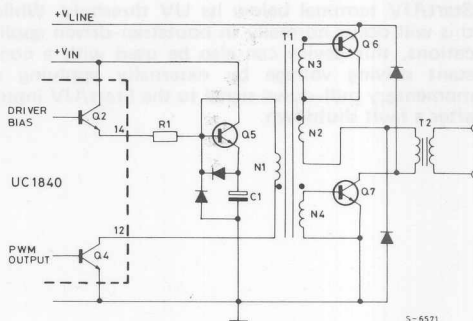
Another application is the two-transistor, off-line, forward converter topology shown in Figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

Fault protection

A significant benefit in using the UC1840 is the multi-faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing

circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

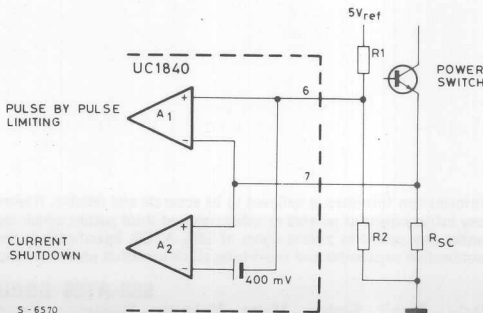
Fig. 14 – Interfacing the UC1840 single PWM output to a two-transistor off-line forward converter which uses proportional base drive.



Current limiting

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in Figure 15. Comparator A1 is delegated to pulse-by-pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by R_{SC} reaches a threshold defined by divider R1, R2, and the 5V reference.

Fig. 15 – Current limiting and overcurrent shutdown are implemented with comparators of different thresholds and a single current sense resistor.



If Driver Bias turn-on is used to pump an increment of charge into an integrating capacitor, and that capacitor voltage is applied to the Reset Terminal, some number of retrys could be programmed to take place before the Reset voltage rises to 3V, which would then lock the output OFF. Since Driver Bias continues to cycle in the latched-off state, the Reset terminal will remain high until it is either remotely pulled low or the input voltage to the controller is interrupted.

Note that an important element in any restart after a shutdown is the lowering of the voltage at the Start/UV terminal below its UV threshold. While this will occur normally in bootstrap-driven applications, this device can also be used with a constant driving voltage by externally applying a momentary pull-down signal to the Start/UV input after a fault shutdown.

CONCLUSION

With the UC1840, power supply designers now have a device specifically developed for off-line, primary control and one which has addressed the problems of operation under less than "ideal" or normal conditions. Not only does this device make it easier to comply with stringent isolation requirements by requiring a minimum of communication between primary and secondary, but it is also ideally suited for powering systems in remote locations where only a simple transmitted pulse is available for power sequencing.

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Since V_C is intended to track the supply's output voltage, the addition of a resistor from pin 6 to V_C will provide some foldback to the current limit characteristic. Since comparator A1 has zero offset voltage, it is activated when the voltage across R_{SC} equals that across R_2 . Comparator A2, with an offset voltage of 400 mV, will activate for over-current shutdown when the voltage across R_{SC} rises to 400 mV higher than the voltage across R_2 . Since the input bias to both comparators is less than 5 μ A, a low-pass filter for noise rejection may be inserted between R_{SC} and the sense inputs. Activation of comparator A2 is defined as an over-current fault and it triggers the Error Latch. Its operation follows.

Fault sequencing

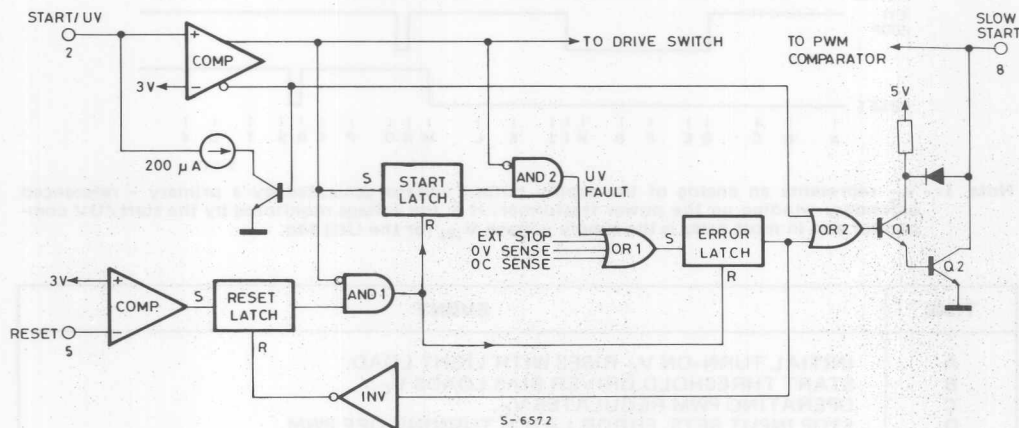
The fault sequencing logic of the UC1840 is shown in Figure 16. Since a fault is defined by this device as an activation of the Error Latch, it makes sense to start here in an attempt to understand this por-

tion of the circuitry. Setting the Error Latch immediately turns on Q1 and Q2, discharging the slow-start capacitor and terminating the PWM output. Note that there is an additional path from the inverted output of the Start/UV comparator through OR2 which keeps pin 8 low. This is to keep the slow-start low during initial turn-on which is not intended to be classified as a fault.

The input to the Error Latch is from OR1 which triggers on signals resulting from four possible events:

- (1) A voltage less than 3V (after prior turn-on) at the Start/UV sense terminal, pin 2.
- (2) A voltage greater than 3V at the Over-Voltage Sense terminal, pin 3.
- (3) A voltage of less than 3V on the Ext. Stop terminal, pin 4.
- (4) An over-current signal resulting in a differential voltage between pins 7 and 6 of greater than 400 mV.

Fig. 16 - Fault sequence logic is designed to insure a complete shutdown and fully controlled restart upon any of four possible fault conditions.



Any of these inputs need only be momentary to set the Error Latch. Transient protection may be necessary to eliminate false triggering, but it can be readily accomplished as all the comparator inputs are high impedances requiring less than 2 μ A of input current, and the 3.0V reference yields a high noise immunity.

The Start Latch can be understood by recognizing that at initial turn-on it is reset with a low output. This prevents AND2 from transmitting a UV fault signal from the Start/UV non-inverting output to the Error Latch. At the start voltage level, defined by a high level on the Start/UV non-inverting output, the Start Latch sets but AND2 still provides no output. Only when the Start/UV input goes low again, with the Start Latch output held high, will AND2 yield an output into the Error Latch.

The status of the Reset terminal, pin 5, determines

what happens after the Error Latch is set. The choices are:

- (1) Latch off and require a recycle of input voltage to restart.
- (2) Continuously attempt to restart.
- (3) Attempt some number of restarts and then latch off.
- (4) Latch off and await a momentary reset pulse to restart.

To examine the operation of the Reset Latch, note that prior to setting the Error Latch, its low output is inverted to hold the reset input to the Reset Latch high. This forces the Reset Latch's output low, regardless of the voltage on pin 5, and, thus, insures no signal out of AND1. With the setting of the Error Latch, the Reset Latch is free to take the

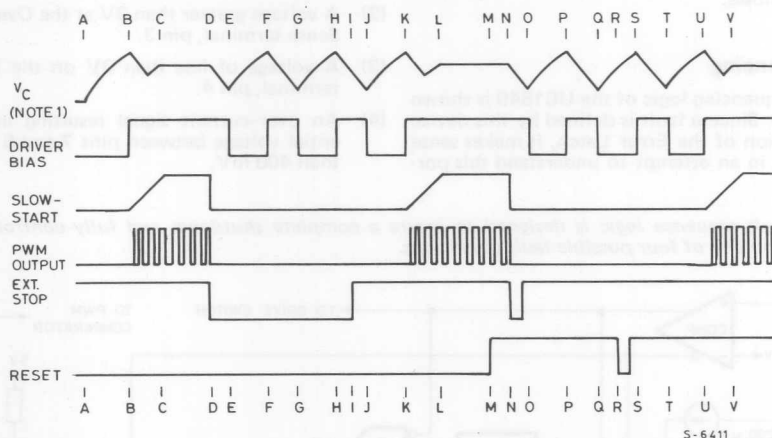
state commanded by pin 5: high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch re-establishing the initial conditions for a

normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, Figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

Fig. 17 - The interrelationship between the functions controlled by the fault sequence logic is illustrated with both static and pulse commands on the ext. stop and reset terminals.



S-6411

Note 1: V_C represents an analog of the supply output voltage generated by a primary - referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and in most cases is the supply voltage V_{IN} for the UC1840.

TIME	EVENT
A	INITIAL TURN-ON V_C RISES WITH LIGHT LOAD.
B	START THRESHOLD DRIVER BIAS LOADS V_C .
C	OPERATING PWM REGULATES V_C .
D	STOP INPUT SETS. ERROR LATCH TURNING OFF PWM.
E	UV LOW THRESHOLD. ERROR LATCH REMAINS SET.
F	START TURNS ON DRIVER BIAS BUT ERROR LATCH STILL SET.
G	V_C AND DRIVER BIAS CONTINUE TO CYCLE.
H	
I	STOP COMMAND REMOVED.
J	ERROR LATCH RESET AT UV LOW THRESHOLD.
K	START THRESHOLD NOW REMOVES SLOW-START CLAMP.
L	RETURN TO NORMAL RUN STATE.
M	RESET LATCH SET SIGNAL REMOVED.
N	ERROR LATCH SET WITH MOMENTARY FAULT.
O	ERROR LATCH DOES NOT RESET AS RESET LATCH IS RESET.
P	V_C AND DRIVER BIAS RECYCLE WITH NO TURN-ON.
Q	
R	RESET LATCH IS SET WITH MOMENTARY RESET SIGNAL.
S	V_C MUST COMPLETE CYCLE TO TURN ON.
T	START AND ERROR LATCHES RESET.
U	NORMAL START INITIATED.
V	RETURN TO NORMAL RUN STATE.



TECHNICAL NOTE 174

OFF LINE SWITCHING POWER SUPPLY USING THE UC3840

INTRODUCTION

This power supply has been designed to provide an easy way to gain familiarity with the operating characteristics of the UC3840 PWM Control Circuit in a practical off-line power supply application. As any switching power supply represents a series of compromises between size, cost, efficiency, performance, and many other variables; no claim is made that this supply optimizes any particular characteristics; only that it provides an easy means to gain an understanding which, hopefully, the designer can use to extrapolate to many specific applications.

This power supply, shown schematically in Fig. 4

implements a 50 watt discontinuous mode flyback power supply with multiple outputs, and features primary-side control with full protection from fault conditions. Additional performance characteristics include simple off-line starting, voltage feed-forward for good line regulation (without feedback across the isolation boundary), pulse-by-pulse current limiting, over- and under-voltage sensing with protective shutdown and automatic restart, and freedom from the need for any circuit adjustments.

For additional information on the operation of the UC3840, reference should be made to TN 168 and data sheet.

POWER SUPPLY SPECIFICATIONS

Input line voltage:	
With 110V jumper:	90 VAC to 130 VAC
With jumper removed:	180 VAC to 260 VAC
Input frequency:	50 or 60 Hz
Switching frequency:	40KHz $\pm$ 10%
Output power:	50W maximum
Output voltages:	5V $\pm$ 5%
	12V $\pm$ 5%
Output current:	2.5 to 5A (5V)
	1 to 2A (12V)
Line regulation:	5V, 0.07% /V
	12V, 0.04% /V
Load regulation:	5V, 2.5%/A
	12V, 2.5%/A
Efficiency @ 50 watts	
$V_{in} = 90$ VAC:	70%
$V_{in} = 130$ VAC:	65%
Output ripple:	5V @ 5A = 200mV
	12V @ 2A = 300mV

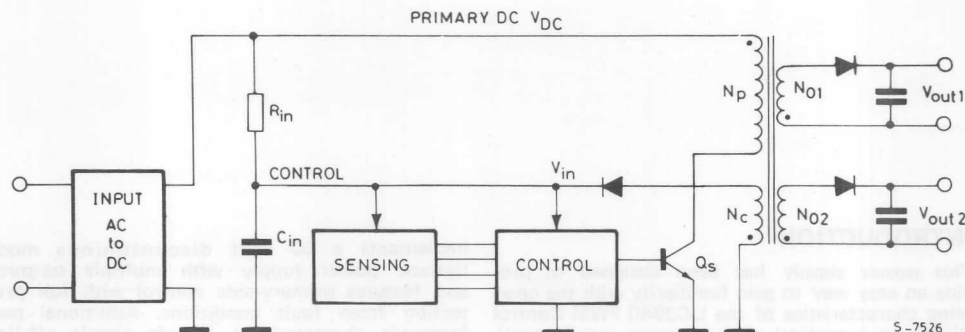
OPERATING PRINCIPLES

In an off-line switching power supply, the input voltage is immediately rectified and filtered, and the resulting DC voltage is chopped at a high frequency. Where 110/220 VAC operation is required, an input voltage doubler configuration is used for 110 VAC input, resulting in a nominal DC input voltage of 310V. The same nominal input voltage is obtained with full wave rectifica-

tion of a 220 VAC line input. High frequency switching allows a very small transformer to be used to efficiently step down to lower output voltages. In the configuration shown in Figure 1 an additional low-voltage winding, N_c , is used to provide continuous operating power for the control and base drive circuits. However, initial energy to start the supply is taken from the line via R_{in} and C_{in} . An additional function on N_c is to provide a primary-referenced feedback voltage that is proportional to the output voltages. This feedback voltage is sensed and regulated by the control circuitry, thereby eliminating the need for feedback across the isolated boundary.

The polarity of the transformer windings identifies this configuration as a flyback supply. When transistor Q_s conducts, all output diodes are reverse biased and the energy is stored in the primary inductance. When Q_s turns off, the voltage polarity of winding N_p reverses (flies back) and the energy is delivered to the output circuits. This circuit operates in the discontinuous mode in which all the energy stored in the transformer inductance is completely transferred to the load during every cycle, i.e. transformer current goes to zero before the end of each cycle. Although this approach yields higher peak current compared to other topologies, it is usually chosen because of its less stringent requirements on the transformer, its faster transient response, and its easier stabilization. To insure discontinuous operation and core reset, the volt-second product across the transformer primary during reset must be allowed to equal or exceed the volt-seconds applied during the on-time of Q_s .

Fig. 1 — Simplified block diagram of a flyback power supply with primary control



DESIGN CONSIDERATIONS

The following description of the design decisions made for this power supply will be with respect to the complete schematic shown in Fig. 4. No significant theoretical discussion is offered and only nominal values are used in the analysis, but hopefully the equations given can be used to either extrapolate to other design problems or to optimize the supply to a particular characteristics.

Input section

Input bridge D1 rectifies the line voltage while resistors R1 and R2 are used to limit the peak charging current to capacitors C1 and C2. The values for C1 and C2 are usually determined by either the ripple voltage allowable for V_{DC} or the minimum hold-up time.

Ripple calculations are worse-case for the 110V voltage doubler configuration where:

RMS line voltage = 90 to 130 VAC
peak no-load input = 253 to 368 volts.

At the minimum line voltage, each capacitor alternately charges to a peak of 126 volts. Allowing for a total input voltage sag at full load of 50 volts, the minimum capacitor voltage must be held to 92 volts. Since each capacitor must provide one-half the energy requirements of the power supply, the required energy for each line cycle is:

$$W_{in} = \frac{\text{Power out}}{\text{Efficiency} \times \text{Frequency}} = \frac{50}{0.7 \times 60} = 1.2 \text{ Joule}$$

and the capacitor value can be calculated from:

$$\frac{1}{2} W_{in} = \frac{1}{2} C_1 (V_{pk}^2 - V_{min}^2) \text{ or}$$

$$C_1 = \frac{W_{in}}{V_{pk}^2 - V_{min}^2} = \frac{1.2}{126^2 - 92^2} = 162 \mu F$$

If, instead of ripple voltage, we choose the input capacitors to hold the input DC above 200 volts for a least two cycles of line drop-out, then:

$$C_1 = \frac{2 (P_o/2) (\text{no. of cycles drop-out}) / f}{\text{Efficiency} (V_{pk}^2 - V_{min}^2)}$$

$$= \frac{2 (25) (2) 1/60}{0.7 (126^2 - 92^2)} = 331 \mu F$$

In this application, 470 μF was picked as a standard size which would allow loose tolerances.

Transformer

A major task with any flyback power supply is the design of the transformer as many tradeoffs are

normally required between regulation, leakage inductance (and corresponding transistor stress), isolation, size, and cost. In this application, the core selected is a Ferroxcube EC35-3C8 which has the following characteristics:

Effective core area, $A_e = 0.84 \text{ cm}^2$
Max flux density, $B_{sat} = 2800 \text{ gauss}$
Bobbin = 35 PC B I

The design starts with a calculation of maximum duty cycle which is defined by the voltage capability of the power switch. This voltage was allocated as follows:

VDC max	= 370V
Reset voltage	= 120V
Leakage inductance spike	= 100V
Max total voltage	= 590V

With a reset voltage of 120V, at minimum input voltage,

$$D_{max} = \frac{120V}{120V + 200V} = 37.5\%$$

The primary inductance can then be calculated as:

$$L_p = \frac{\text{Efficiency}}{2 P_o f} (V_{in \text{ min}} \times D_{max})^2 =$$

$$= \frac{0.7 (200 \times 0.375)^2}{2 \times 50 \times 40 \times 10^3}$$

$$L_p \approx 1 \text{ mH}$$

The peak current at full load is:

$$I_p = \frac{2 P_o}{\text{eff} (V_{in \text{ min}} \times D_{max})} =$$

$$= \frac{2 \times 50}{0.7 \times 200 \times 0.375} = 1.9 \text{ A}$$

The maximum energy storage requirement within the primary is calculated on the basis of maximum current, in this case assumed to be short circuit current = 120% $\times I_p$ or 2.3A.

$$W = \frac{1}{2} L I_{sc}^2 = \frac{1}{2} (1 \times 10^{-3}) (2.3)^2 = 2.65 \text{ m Joule}$$

The equation defining energy storage in an inductor is:

$$W = \frac{1}{2} \frac{B A_c H l_e \times 10^{-8}}{0.4 \pi} \text{ Joules}$$

$$H_{le} = (0.4\pi) \frac{2W \times 10^8}{BA_c} =$$

$$= \frac{0.4\pi \times 2 \times 2.65 \times 10^{-3} \times 10^8}{2800 \times 0.84} = 282 \text{ Gilberts}$$
$$N_p = \frac{H l_e}{0.4 \pi I_{sc}} = \frac{282}{0.4 \pi \times 2.3} = 98 \text{ turns}$$
$$H = \frac{B}{\mu} = 2800 \text{ Oersteds}$$
$$I_g = 0.4 \pi \frac{NI}{H} = \frac{0.4 \pi (98) 2.3}{2800} = 0.1 \text{ cm}$$
$$N_s = \frac{N_p (V_o + \text{rectifier } V_f) (1 - D_{\max})}{V_{in (\min)} D_{\max}}$$

First winding — primary — 97 turns, AWG 24
Second winding — 5 volt — 4 turns, 4 parallel
AWG 22
Third winding — 12 volt— 9 turns, 2 parallel
AWG 22
Last winding — control — 9 turns, AWG 24 evenly
spaced along the full bobbin length

In this application, the peak switch current is 2.3 amps and the peak collector voltage will be approximately 590 volts including the spike caused by leakage inductance. The switching transistor selected is the MJE13005 which has the following characteristics relative to this application:

$$\begin{aligned} BV_{ce0} &= 400V \\ BV_{cer} &= 700V \\ I_c \text{ (cont)} &= 4A \\ h_{fe} &= 8 - 40 @ 2A \\ t_s &= 1.5\mu s \\ t_r &= 0.28\mu s \\ t_f &= 0.25\mu s \end{aligned}$$

While offering inexpensive, high-voltage switching, the MJE13005 needs some support to provide adequate base drive and minimize storage time. This is readily accomplished with the circuitry shown in Figure 2. Prior to obtaining a

start-up signal, the Drive Bias transistor in the UC3840 is off insuring that there is no quiescent current being drawn by any of this interface circuitry. At start-up, the Drive Bias switch turns on providing a pull-up for the UC3840's PWM output. The current through R16 is multiplied by the gain of Q1 to provide a forward base drive in excess of 250mA for the power switch Q3. Diodes D5 and D6 form a Baker clamp to keep Q3 out of hard saturation and improve turn-off, especially at lower collector currents.

Transistor Q2, driven on by the turn-off of Q1, provides a low-impedance path for reverse base current of Q3, and together with the use of the Baker clamp, results in a storage time for Q3 of less than 800nsec.

Snubbing circuits

There are two snubber circuits incorporated into this supply. The network of C12, D7, and R27 is used for load line shaping of transistor Q3 by delaying the voltage rise at the collector of Q3 while the current falls at turn off.

The values for the components in this network are calculated as follows:

$$C12 = \frac{I_{sc} t_f}{2 V_{in(max)}} = \frac{2.3 \times 0.25 \times 10^{-6}}{2 \times 370} \approx 680pF$$

The resistor R27 is selected to discharge C12 with a time constant of one-half the minimum on time, which — under short circuit conditions — is approximately 2.5μs.

$$R27 = \frac{t_{on(min)}}{2C12} = \frac{25 \times 10^{-6}}{2 \times 680 \times 10^{-12}} \approx 1.8K\Omega$$

The power dissipated in this resistor is

$$P = \frac{1}{2} C12 (V_{in(max)})^2 f = \frac{1}{2} (680 \times 10^{-12}) (370)^2 40 \times 10^{-3}$$

$$P \approx 2 \text{ watts}$$

The second network of R26, C11, and D2 limits the voltage spike at turn off caused by the leakage inductance of the power transformer. The energy stored in this inductance is transferred into C11 via D2 after the power switch turns off and the voltage rises above the supply plus reset voltage.

C11 is defined by:

$$C11 = \frac{L_e I_{sc}^2}{(V_{reset} + \Delta V_{pp})^2 - V_{reset}^2}$$

Where L_e = Leakage inductance ($\approx 50\mu H$)
 V_{reset} = Reset voltage across transformer (120V)
 V_{pp} = Allowable leakage inductance Voltage spike (100V)

$$\therefore C11 = \frac{50 \times 10^{-6} (2.3)^2}{(120 + 100)^2 - 120^2} = 0.0078 \approx 10nF$$

Resistor R26 is selected to discharge C11 during the remainder of the period leaving a residual voltage equal to the reset voltage at the time turn-off next occurs.

$$R26 = \frac{(V_{reset} + \Delta V_{pp}) 0.63 \tau}{\Delta V_{pp} C11} = \frac{220}{100} \frac{0.63 (25 \times 10^{-6})}{(0.01 \times 10^{-6})} = 3.5K\Omega$$

In this application, R26 was increased to 4.7k due to second order effects such as reverse recovery of D2 which aids in discharging C11.

The power loss in R26 comes from the energy stored in the leakage inductance which is

$$P = \frac{1}{2} L_e I_{sc}^2 f = \frac{1}{2} 50 \times 10^{-6} (2.3)^2 40 \times 10^{-3}$$

$$P \approx 5.3 \text{ watts}$$

but here again, second order effects tend to reduce this value to less than 3 watts in this power supply.

Operating frequency

The frequency is set by R14 and C4 as

$$f = \frac{1}{R_T C_T} = \frac{1}{R_{14} C_4} = \frac{10^3}{12 \times 0.0022} \approx 40kHz$$

Supply start-up

The supply must reliably start with V_{DC} minimum = 250V. The value of R3 + R4 is defined by the total current requirement of the control electronics prior to start. If a start threshold of 12 volts is assumed, total control current is:

UC3840 max	= 7.0mA
R7 + R8	= 0.70mA
R10 + R11	= 0.27mA
C4 charging current	= 0.40mA
R17 + R18	= 0.22mA
Total Turn-On Current	8.59mA

$$\text{and } R3 + R4 = \frac{250 - 12}{8.59} = 27K\Omega$$

Note that R3 and R4 also provide a bleeder path to discharge C1 and C2.

Once start-up is initiated, the control current becomes:

UC3840 max	= 15mA
R16	= 6mA
Q3 Ib (x 0.375 duty cycle)	= 94mA
Total run current	= 115mA

This current must come from C3 until power is available from control winding, N4. This, in conjunction with the start-up time, defines a minimum value for C3.

Although a small soft-start capacitor is incorporated in this supply, its time constant is much shorter than the time to charge the output capacitors with the duty cycle defined by the ramp waveform and the pulse-by-pulse current limit. With the supply fully loaded, start up takes approximately 5msec. During this time, the voltage on C3 cannot fall below the under-voltage threshold.

In defining the start and UV thresholds, one other consideration is the state of the error amplifier. As defined further below, the error amplifier is going to force V_C to 12 volts. If the start threshold is set above this value, the start signal will release the soft-start clamp and arm the driver bias but no PWM output will appear until V_C droops below 12 volts and the output of the error amplifier goes high. To insure soft-start action, the start threshold has been set at 11 volts and the under-voltage level is 8 volts.

Now the value for C3 can be determined from:

$$C3_{(min)} = \frac{I_{(start)} t_{on}}{\Delta V_C} = \frac{(115 \times 10^{-3}) (5 \times 10^{-3})}{(11 - 8)} = 192 \mu F$$

The start and under-voltage thresholds are defined by R7 and R8 conjunction with the 3 volt threshold and the hysteresis current of the comparator on pin 2 of the UC3840. As the voltage rises on pin2, that pin is sinking 200 μ A of current causing an added voltage drop across R7. When pin 2 reaches 3 volts, turn-on is initiated and — at the same time the hysteresis current is removed causing the voltage at pin 2 to jump above 3 volts.

Now, as the power supply attempts to start, the voltage on pin 2 falls and, if it reaches 3 volts from this direction, an under-voltage fault is sensed.

The start voltage at V_C is defined by:

$$V_{C(start)} = \frac{3V (R7 + R8)}{R8} + 0.2mA (R7) = 11V$$

while the under-voltage threshold is:

$$V_C (UV \text{ fault}) = \frac{3V (R7 + R8)}{R8} = 8V$$

This second equation may be subtracted from the first to yield $R7 = 15K\Omega$, which then defines $R8 = 9.1K\Omega$.

An over-voltage fault in terms of V_{DC} can be calculated by equation:

$$V_{DC} (OV \text{ fault}) = 3V \frac{(R5 + R6)}{R6} = 400V, \text{ or}$$

$$R5 = 132 R6$$

Small capacitors (10nF) have been added to both comparator inputs to minimize noise sensitivity.

Feed-forward

This function provides a variable-slope ramp waveform on pin 10 which is one of the inputs to the PWM comparator. This signal is compared with the output from the error amplifier on pin 1, and the pulse width is defined by the time it takes the ramp to rise to the level of the error amplifier's output. If the ramp slope is made proportional to the DC input voltage, a rising input voltage will immediately increase the ramp slope, and correspondingly reduce the pulse width with no change required from the error amplifier's output. The result will be a constant volt-second product delivered to the transformer primary resulting in good open-loop line regulation.

The design procedure used to define the ramp characteristics is to set the ramp slope such that it reaches its peak value at a time equal to the maximum pulse width allowed by the transformer design. This was set at 43% with minimum input voltage and a potential shorted output. The time for the ramp to go from its minimum to maximum value is then:

$$t_{on(max)} = \frac{0.43}{f} = \frac{0.43}{40 \times 10^3} = 10.75 \mu sec$$

and the slope is:

$$\frac{dv}{dt} (min) = \frac{V_{pk} - V_{valley}}{t_{on(max)}} = \frac{4.2 - 0.5}{10.75} = 0.344 V/\mu sec$$

and since the slope is determined by:

$$\frac{dv}{dt} = \frac{V_{DC}}{R15 C8}$$

$$\therefore R15 C8 = \frac{200V}{0.34V/\mu s} = 581\mu sec$$

With the knowledge that the ramp generator has greatest linearity with currents in the 100 μ A to 300 μ A range, we can pick:

$$R15 = 1.5M\Omega \text{ and } C8 \cong 390pF.$$

Duty cycle clamp

The above analysis has provided a maximum duty cycle of 43% at minimum operating voltage. When the AC line voltage is removed, however, the input voltage will fall below 200 volts with the supply still running. As this voltage falls, the ramp slope will reduce and at the same time the error amplifier output will increase in an attempt to maintain regulation. This could extend the pulse width beyond 43% except for the action of the duty cycle clamp divider of R19 and R20 which is set to provide 3.9V at pin 8 with $V_{DC} = 200V$. Therefore, as V_{DC} falls, the voltage on pin 8 will also fall, taking command away from the error amplifier and maintaining a constant pulse width until the Under-Voltage sensing circuit gives a shutdown command.

Voltage control

In this power supply, output voltage regulation is controlled from the primary side by sensing V_C with R10 and R11 and closing a control loop with the error amplifier and 5V reference in the UC3840. The output voltage is then:

$$V_O (5V) = \left(\frac{N2}{N4} \right) V_{ref} \left(\frac{R10 + R11}{R11} \right)$$

Although the UC3840 optimizes this approach by the use of feed-forward which provides first-order automatic line regulation, there will still be inaccuracies caused by inadequate coupling between the windings, IR drops within the windings, and unequal losses in the rectifiers. If greater voltage accuracy is required, the feedback loop must be connected directly to one of the outputs with either an optical coupler or the UC1901 Isolated Feedback Generator used to maintain isolation.

The gain and phase plots for this supply are shown in Figure 3. Overall loop stability is aided by the fact that a discontinuous-mode flyback topology is inherently a single pole system defined by the output load. Its transfer function, excluding the error amplifier, is shown by the dashed curve of Figure 3. The DC gain from the modulator input v_C , to the output, v_O , is:

$$\frac{v_O}{v_C} = K \sqrt{\frac{T R_{L \min}}{2L_P}}$$

where K is defined by the feed-forward slope as

$$K = \frac{(\text{Max duty cycle}) (V_{in \min})}{\text{Ramp peak} - \text{Ramp valley}} = \frac{0.43 \times 200}{4.2 - 0.5}$$

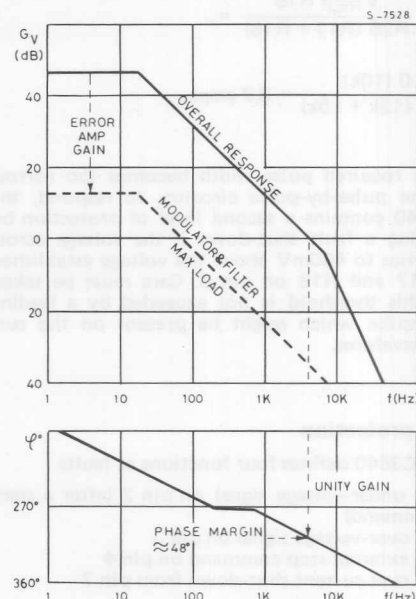
and the minimum load resistance reflected to the primary control supply is:

$$R_{L \min} = \frac{V^2}{P_{O \max}} = \frac{12^2}{50} = 2.88\Omega$$

$$\therefore \frac{v_O}{v_C} = \frac{0.43 \times 200}{4.2 - 0.5} \sqrt{\frac{25 \times 10^{-6} \times 2.88}{2 \times 1 \times 10^{-3}}} =$$

$$= 4.41 = 13db$$

Fig. 3 — Power supply loop gain and phase



The effective output capacitance, also reflected to the control supply, is:

$$\begin{aligned} C_E &= C14 \left(\frac{N2}{N4} \right)^2 + C13 \left(\frac{N3}{N4} \right)^2 + C3 \\ &= 4700 \left(\frac{4}{9} \right)^2 + 2200 \left(\frac{9}{9} \right)^2 + 200 \\ &= 3328\mu F \end{aligned}$$

The yields an output pole at

$$f_1 = \frac{1}{2\pi R_L C_E} = \frac{10^6}{6.28 (2.88) 3328} = 16.6\text{Hz}$$

The error amplifier is set up for an added DC gain of approximately 35db and a second pole at 8kHz - a frequency well above the overall unity gain point and yet below the roll-off frequency of the error amplifier.

Current limiting

The UC3840 limits current through the power switch, Q3, by sensing the voltage across R25. Pulse-by-pulse current limiting is defined by the divider R17, R18, and the value of R25 as:

$$I_{sc} = \frac{V_{REF} R18}{R25 (R17 + R18)} = \frac{5.0 (10k)}{1\Omega (12k + 10k)} = 2.2 \text{ amps.}$$

If the required pulse width becomes too narrow for the pulse-by-pulse circuitry to respond, the UC3840 contains a second level of protection by initiating a fault shut-down if the voltage across R25 rises to 400mV above the voltage established by R17 and R18 on pin 6. Care must be taken that this threshold is not exceeded by a leading edge spike which might be present on the current waveform.

Fault protection

The UC3840 defines four functions as faults.

1. An under-voltage signal on pin 2 (after a start command)
2. An over-voltage signal on pin 3
3. An external stop command on pin 4
4. An over current shut-down from pin 7

Any of these functions will initiate a complete shutdown of the controller with restart defined by the voltage on the reset terminal, pin 5.

If pin 5 is high or open, any fault will latch the supply off and it can only be restarted by reducing the input voltage to zero or by momentarily pulling pin 5 low. Alternatively, grounding pin 5 will cause an automatic restart after any fault shut-down.

CONSTRUCTING THE KIT

It is assumed that the user possesses reasonable electronic assembly skills and therefore detailed

step-by-step instructions have not been considered necessary. Rather, a general assembly procedure is outlined below which, if followed carefully, should offer no problems. Assembly starts by properly orienting the PC board with the assembly drawing shown in Figure 5. This drawing is of the component side of the board - etch side down - with the "Warning - HighVoltage" label at the lower left hand edge.

Test and tie points

Pads have been provided on the PC board for input and output connections and for many internal test points so that complete operation of all portions of the control circuitry can be evaluated. These points are noted in Figure 5 and are listed below:

AC input	(2 pads)
DC input	{ (2 pads each - note that the commons may be separated for alternate polarities)
+ 12V output	
+ 5V output	

H.V. Switching	
Transistor	(3 pads)

Note: 600V pulses will appear at the collector.

BE CAREFUL OF THIS TEST POINT.

Control Voltage V_C	IC pin 15
Primary Common	IC pin 13 (2 pads)
E/A Compensation	IC pin 1
5.0V Reference	IC pin 16
E/A input	IC pin 17
Drive Bias	IC pin 14
PWM Control	IC pin 12
Ramp Waveform	IC pin 10
S/S Duty Cycle Limit	IC pin 8
Oscillator Frequency	IC pin 9
C/L Limit Sense	IC pin 7
C/L Threshold	IC pin 6
Reset input	IC pin 5
Ext. Stop Input	IC pin 4
OVP Sense Input	IC pin 3
UV/Start Input	IC pin 2

No connections to these points have been included in this kit. It is suggested that the user either supply terminals or solder in small stubs or loops of bus wire so that connections to these test points can easily be made on the component side of the PC board with scope probes or other test instrumentation leads.

Jumpers

There are four jumpers required which are also not included in this kit. Use solid bus wire or a section clipped from the ends of the small resistors. These jumpers are:

AC input jumper for 110V operation
(leave out if 220 VAC is to be used)
PWM jumper to pin 12
UV/start jumper to pin 2

Reset jumper on pin 5

(leave out if it is desired to latch the supply off after any fault)

Note that there is nothing connected to pin 4. A low signal here will shut down the supply.

Small signal diodes

The seven small axial lead diodes, D2 through D8 should next be installed insuring correct polarity as shown in Figure 5.

Passive devices

Install the low-power resistors and small capacitors first. Follow with the four high-power resistors, R3, R4, R26 and R27. When inserting R26, keep the body of the resistor $\approx \frac{3}{4}$ inch above the PC board. This resistor will get hot and it is best to have it above, rather than next to C11. At this time, the input diode bridge, D1, and the IC socket can be inserted. Note that pin 1 of the UC3840 is to the front of the PC board.

Large components

Assembly can be completed by installing the remaining components as follows:

- a. Two small signal transistors, Q1 and Q2
- b. Transformer
- c. Electrolytic capacitors: C1, C2, C3, C13 and C14. Check polarity against signs of foil side of PC board.
- d. Power transistor Q3 inserts with its front to the left, or input, inside of the PC board. Insertion is easier if the heat sink is clipped on first.

NOTE: THIS HEAT SINK IS AT THE SAME POTENTIAL AS THE COLLECTOR AND WILL HAVE UP TO 600 VOLTS PRESENT: KEEP IT CLEAR OF OTHER COMPONENTS, TEST LEADS, AND YOUR FINGERS.

- e. Install the 5 volt output rectifier, D9 with its front facing the right, or output side of the board. It also gets a clip-on heat sink.

Check to see that all components are installed and match the drawing of Fig. 5. Insert the UC3840 into the socket.

CHECKOUT PROCEDURES

With the power supply fully assembled, the following checkout procedure is recommended before any input voltage is applied. This procedure is also useful for trouble-shooting a unit which is not operating properly. Checkout will be aided if the user has installed test points at all indicated positions in the PC board. Reference should be made to Figure 5 for test point locations.

1. Insure that there is no AC input voltage applied
2. Double check all connections including diode and capacitor polarities. Insure that the UC3840 is correctly inserted into the socket.
3. Connect a minimum load on one or both outputs equivalent to 25 watts total. i.e., 2Ω on the 5V output and 12Ω on the 12V output. Be careful of the heat from these loads.
4. Install a temporary jumper shorting the base and emitter of Q3 together. Use test points provided on PC board.
5. Connect a 0 to 30 volt, 500mA lab supply to simulate the control voltage, V_C . Connect the positive lead to IC-15 and ground to IC-13. Note that IC-13 will be the ground reference point for all primary side measurements. Set V_C = Zero volts and add a $1k\Omega$, $\frac{1}{2}$ W resistor in shunt across the power supply terminals.
6. Increase V_C to 10 volts and check the following:
 - a. IC-16: should have 5V if the reference is working.
 - b. IC-2: Should be 2.3V if hysteresis current is on.
 - c. IC-14: Should be $< 0.1V$ as Driver Bias is off.
7. Increase V_C to 14 volts and check the following:
 - a. IC-2: Should be 4.7 volts if hysteresis current is off.
 - b. IC-14: Should be 12 volts with Driver Bias on.
 - c. IC-9: Oscillator should show 40kHz exponential waveform.
 - d. Return V_C to Zero volts but leave connected.
8. Apply the high voltage, V_{DC} . This can be done either with a DC lab supply with 300V capability or the input AC line voltage.

A fuse rated at no more than two amps should be in series with the input line to prevent excessive damage in the event of a failure.

NOTE: BE SURE TO USE AN ISOLATION TRANSFORMER WHEN LINE POWER IS USED AS PRIMARY GROUND IS ONE SIDE OF THE LINE.

An AC variac will also be helpful in varying the input voltage.

If a DC power supply is used, connect the positive line to the V_{DC} test point at the top of the board. The negative line will connect to ground on IC-13. Insure that the base-emitter short is still connected to Q3.
9. With V_{DC} = 200 volts, set V_C = 10 volts and check the following:
 - a. IC-14: Should be $< 0.1V$ if Driver Bias is off
 - b. IC-8: Should be $< 0.1V$ if Slow Start clamp is on.
 - c. IC-6: Should be 2.3V to establish current limit threshold.

- WARNING: PULSES UP TO 600V ARE ON Q3'S COLLECTOR

Normal power supply evaluation tests of line and load regulation, etc., may now be conducted.

NOTE: In experimenting with this supply, the most probable mode of failure is the shorting of the high-voltage transistor, Q3. Should this occur, transistor Q2 will also go. A two amp input fuse will normally protect the input diodes, R1,R2 and the current sense resistor, R25, although these should be checked before reapplying power. Diodes D5 and D6 are normally adequate to protect Q1 and the IC.

ICs		Resistors		Miscellaneous
U1	UC3840N	R1, R2	1 Ω , ½W	HS1, HS2, Heat Sink Thermalloy 6043
		R3	15k, 2W	TI Transformer
Transistors		R4	12k, 2W	Coilcraft, E - 4140 - B
Q1, Q2	2N2222	R5	750k	
Q3	MJE 13005	R6	5.6k	
		R7	15k	
Diodes		R8	9.1k	
D1	VM68 Bridge	R9	unused	
D2, D6, D7	1N3614	R10	2.67k, 1%	
D3, D4	1N3612	R11	17.8k, 1%	
D5	1N4946	R12	1.5M	
D8	UES1103	R13, R14	12k	
D9	USD735	R15	1.5M	
		R16	1.5k	
Capacitors		R17	12k	
C1, C2	470 μ F, 250V	R18	10k	
C3	200 μ F, 25V	R19	750k	
C4	2200pF, 10%	R20	15k	
C5, C6	10nF, 50V	R21	33 Ω , ½W	
C7	22pF	R22	15k	
C8	390pF, 10%	R23	4.7k	
C9, C10	10nF, 50V	R24	2.0k	
C11	10nF, 400V	R25	1.0 Ω , 1W	
C12	680pF, 800V	R26	4.7k, 4W	
C13	2200 μ F, 16V	R27	1.8k, 2W	
C14	4700 μ F, 10V			

Fig. 4 — UC3840 PWM control circuit

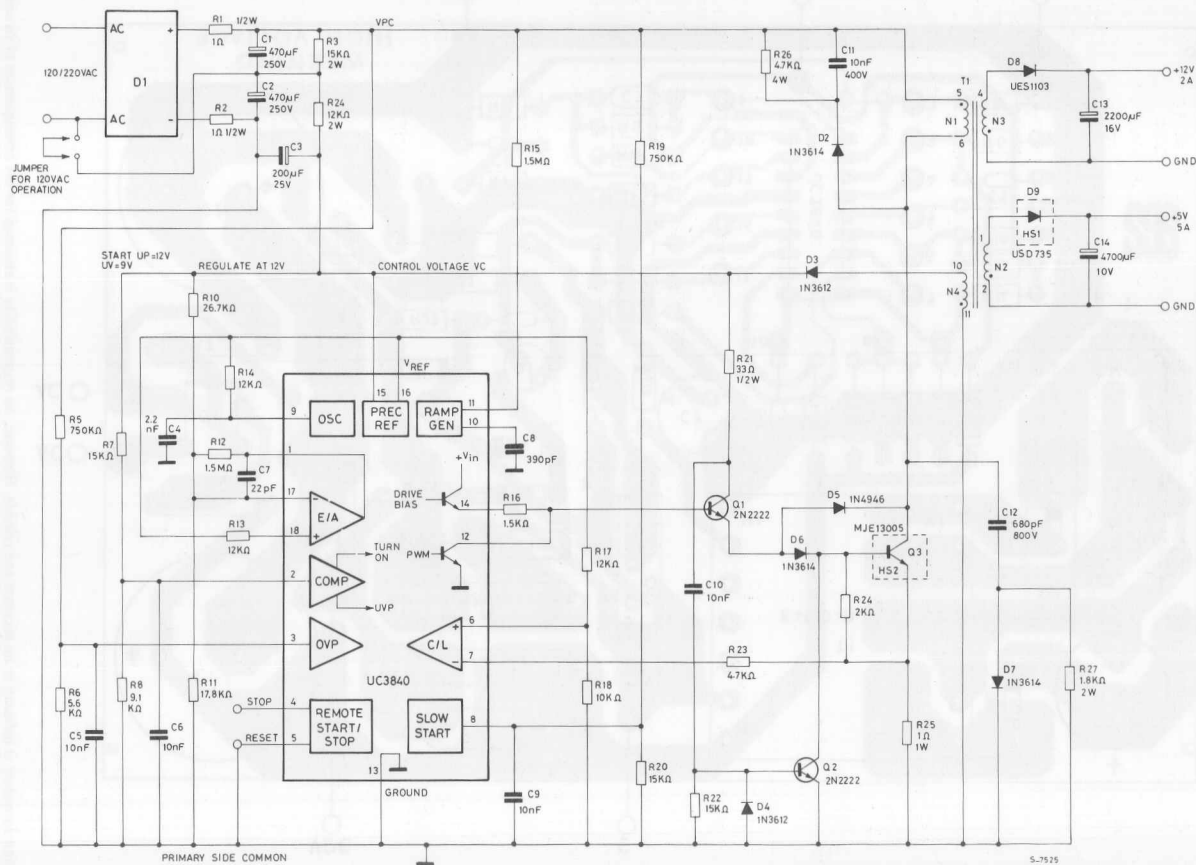
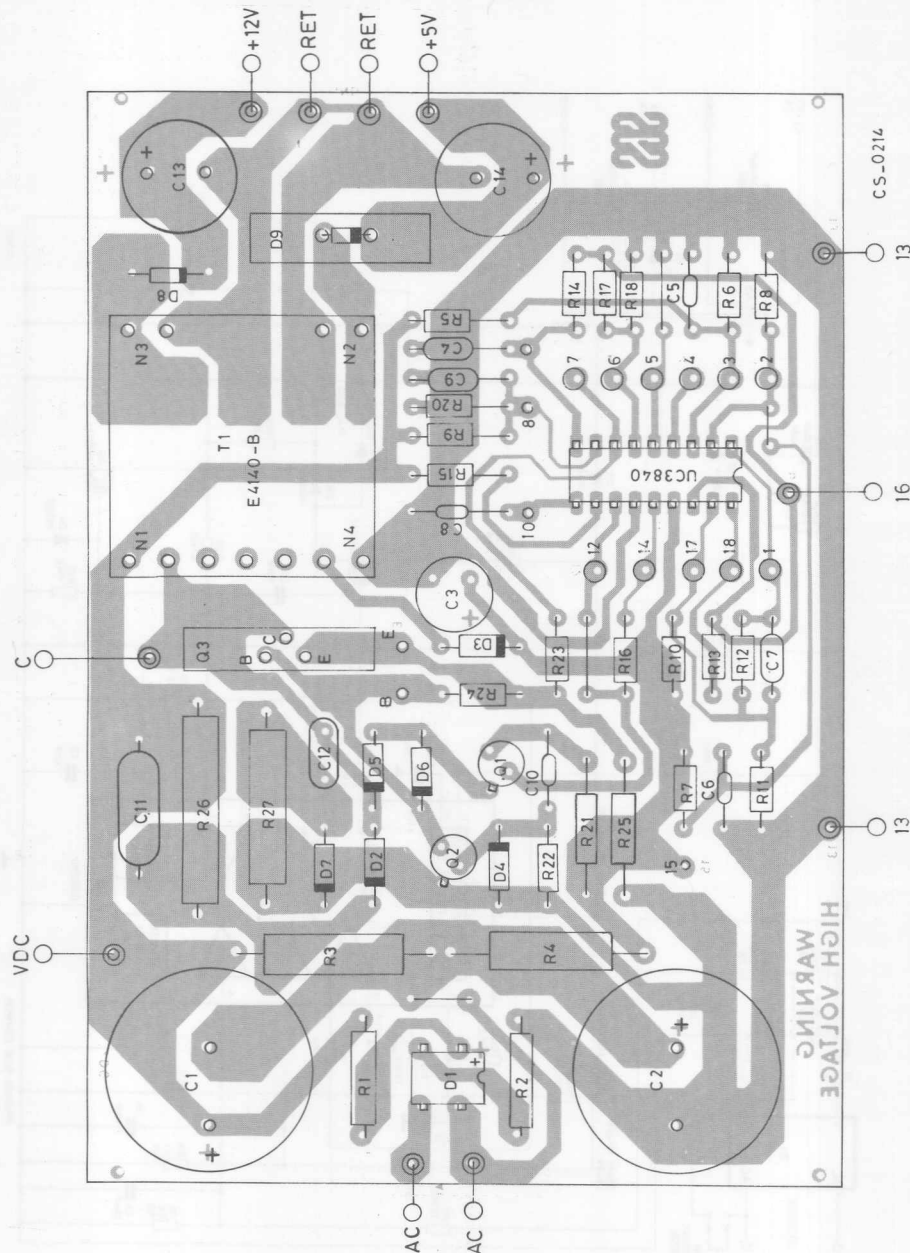


Fig. 5 — P.C. board components layout of the Fig. 4 (1 : 1 scale)



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